

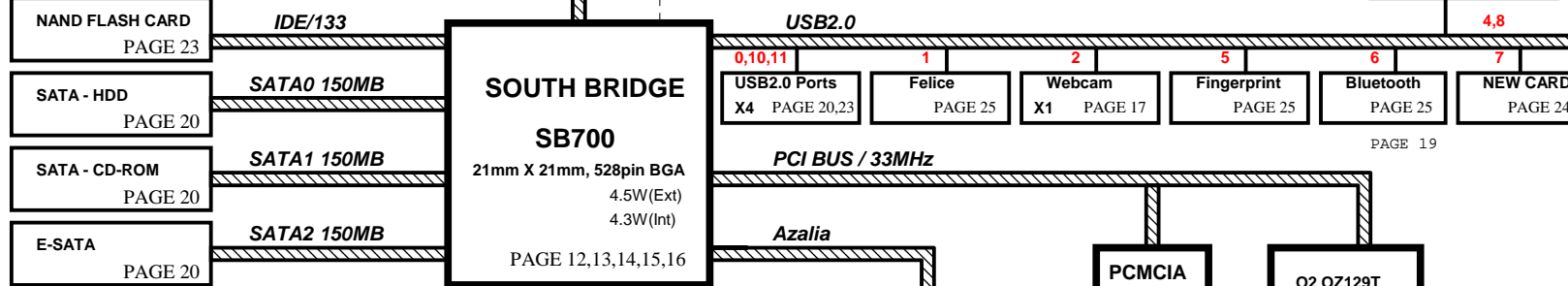
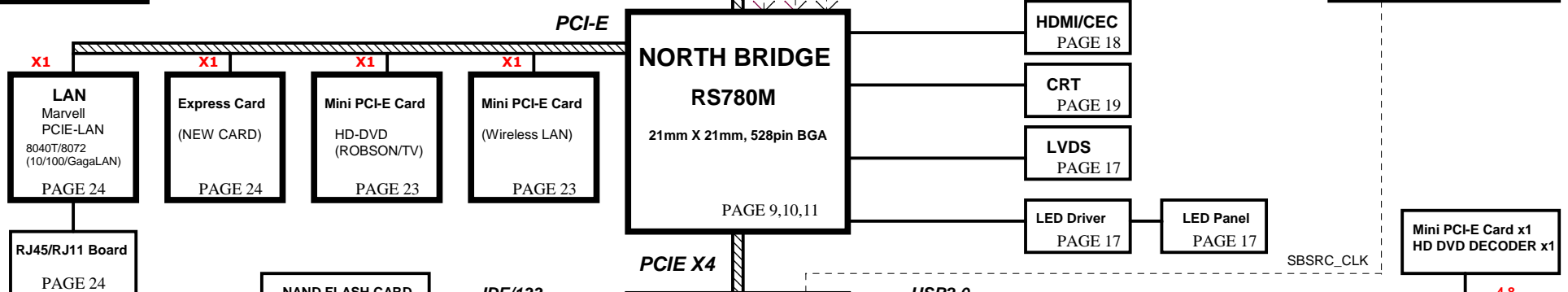
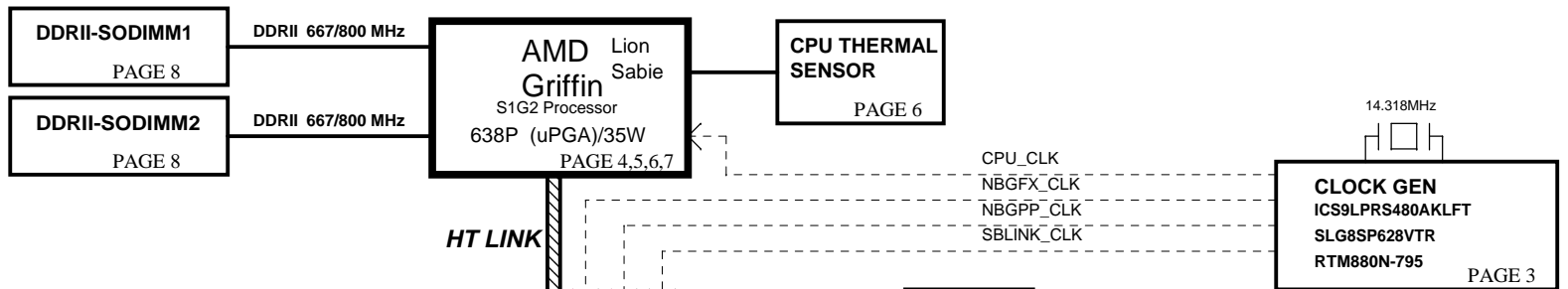
BU2 SYSTEM DIAGRAM



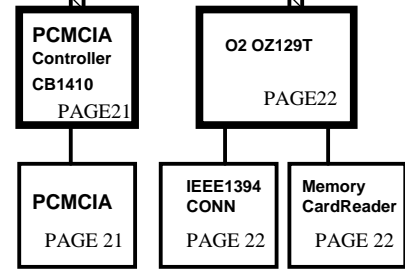
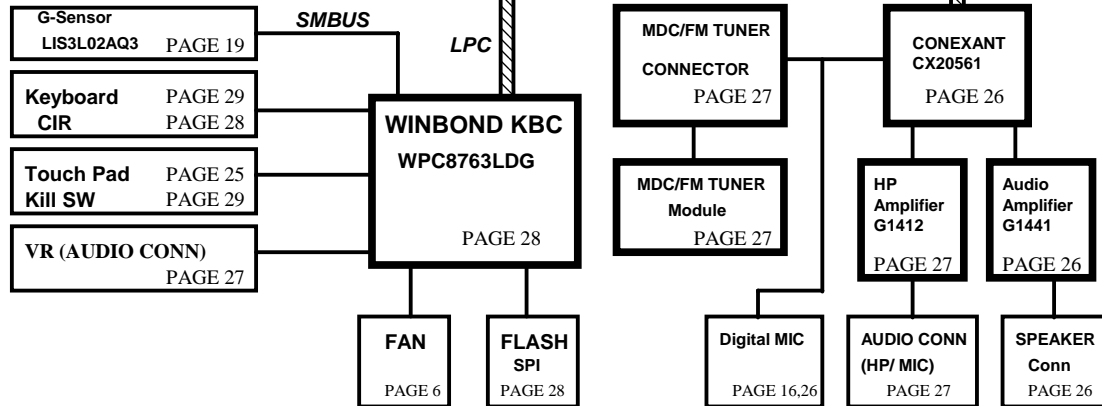
01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT



- SYSTEM CHARGER (ISL88731) PAGE 30
- SYSTEM POWER ISL6237IRZA-T PAGE 31
- CPU CORE ISL6265A PAGE 32
- VCCP +1.1V AND +1.2V (MAX8717) PAGE 33
- DDR II SMD DR_VTERM 1.8V/1.8VSUS (TPS51116REGR) PAGE 34
- DISCHARGE 1.5/1.25/1.2/1.1V PAGE 35



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTE#	OZ129T
REQ1# / GNT1#	AD18	INTF#	CB1410

PROJECT : BU2
Quanta Computer Inc.

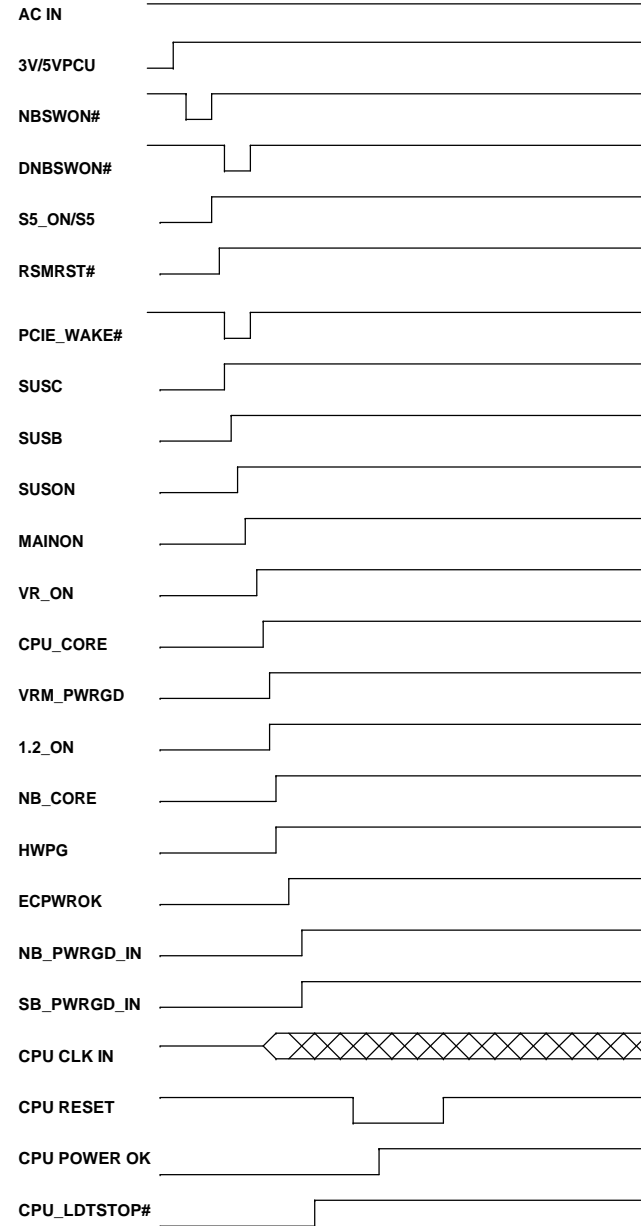
Size Custom Document Number
NB4 **BLOCK DIAGRAM** Rev 1A

Date: Wednesday, January 30, 2008 Sheet 1 of 35

INDEX

PAGE#	DESCRIPTION	NOTE
1	SCHEMATIC BLOCK DIAGRAM	
2	SYSTEM INFORMATION	
3	CLOCK GENERATOR_SLG8SP628	
4	S1G2 HT I/F 1/4	
5	S1G2 DDRII MEMORY I/F 2/4	
6	S1G2 CTRL & DEBUG 3/4	
7	S1G2 PWR & GND 4/4	
8	DDR2 SODIMMS: A/B CHANNEL	
9	RS740/RS780-HT LINK/PCIE I/F 1/4	
10	RS740/RS780-SYSTEM I/F 3/5	
11	RS740/RS780-POWER5/5	
12	SB700-PCIE/PCI/CPU/LPC 1/4	
13	SB700-ACPI/GPIO/USB 2/4	
14	SB700-ACPI/GPIO/USB 2/4	
15	SB700-PWR/DECOUPLING 4/4	
16	SB700-STRAPS & PWRGD	
17	LCD/LED PANEL/LID/CAMERA	
18	HDMI/HDMI-CEC(R5F211A)	
19	CRT & G-SENSOR(LIS3L02A)	
20	SATA HDD/ODD & ESATA/USB	
21	PCMCIA(CB1410) -OPTION	
22	OZ129T(5IN1/1394)	
23	MINI CARD & NAND FLASH CARD	
24	NEW CARD & RJ45 BOARD/BEEP	
25	TP/FP/BT/PB/FELICA/MMB CONN	
26	CONEXANT(CX205601)/SPK/AMP	
27	JACK/VR/FM/MIC/MDC/AMPLIFIER	
28	EC(KBC)-WPCPC8763/WPC8769	
29	KEYBOARD/LED/KILL SW/HOLE	
30	CHARGER (ISL6251A)	
31	SYSTEM 5V/3V (ISL6237)	
32	AMD GRIFFIN (ISL6265)	
33	+NB_CORE (RT8202)	
34	DDR 1.8V(TPS51116)	
35	DISCHARGE (1.25V/1.5V)	

Power Sequence



02

SB700 SM BUS

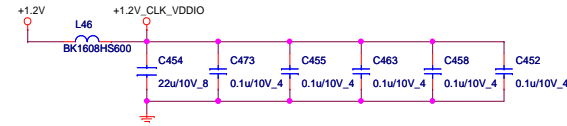
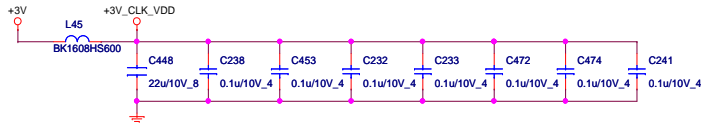
SB700 SMBUS	SMBUS Function Define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card/New Card (+3VS5)
SMBCLK2 SMBDAT2	HDMI CEC (+3VS5)

KBC(EC) SM BUS

KBC SMBUS	SMBUS Function Define
MBCLK MBDAT	BATTERY (+3VPCU)
2ND_MBCLK 2ND_MBDATA	CPU THER / SENSOR/EC (+3V/PCU)
3ND_MBCLK 3ND_MBDATA	HDMI CEC / TOUCH SEN(+3VS5)



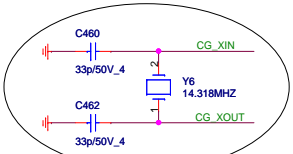
PROJECT : BU2
Quanta Computer Inc.



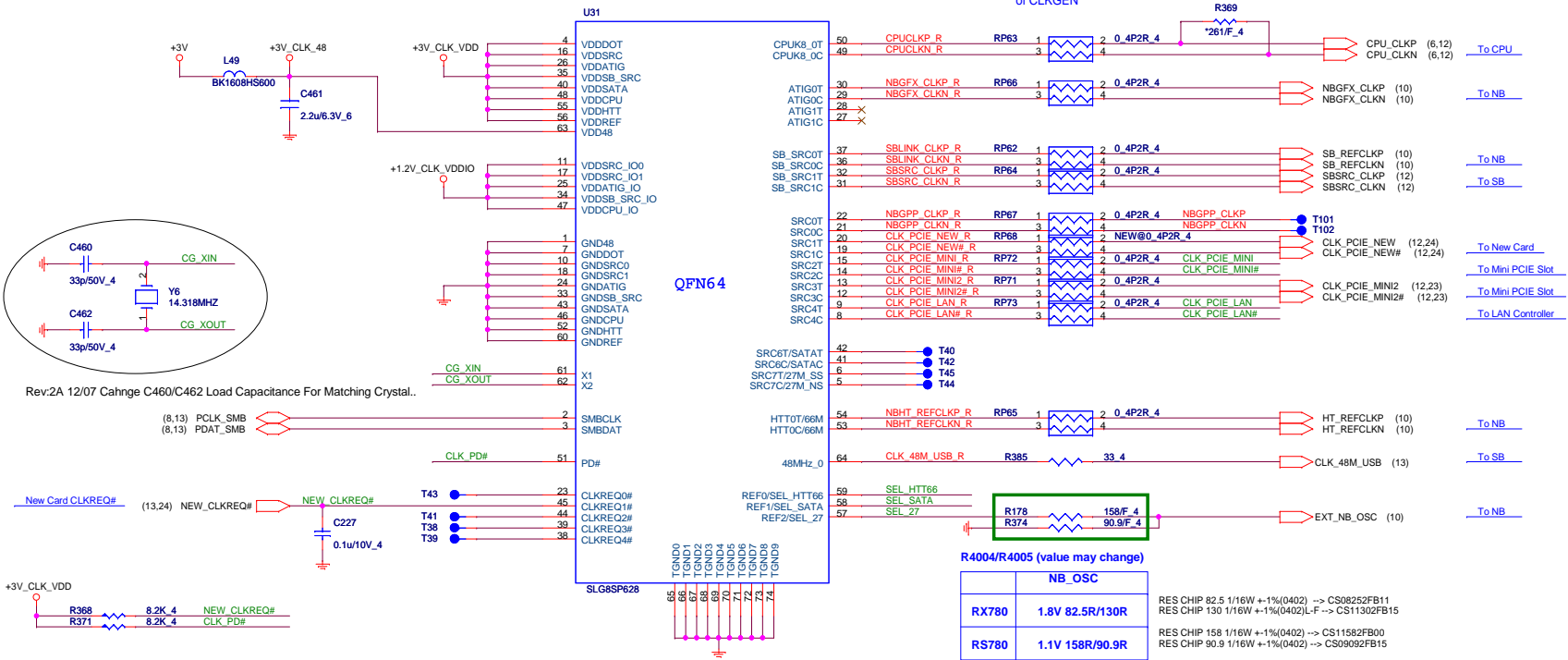
ICS9LPRS480 P/N :
 SLG8SP628 P/N : AL8SP628000
 RTM880N-796 P/N : AL00880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN



Rev.2A 12/07 Cahnge C460/C462 Load Capacitance For Matching Crystal..



NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

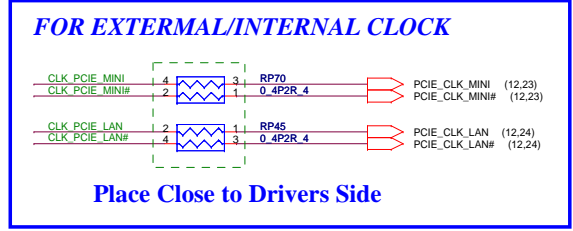
R4004/R4005 (value may change)

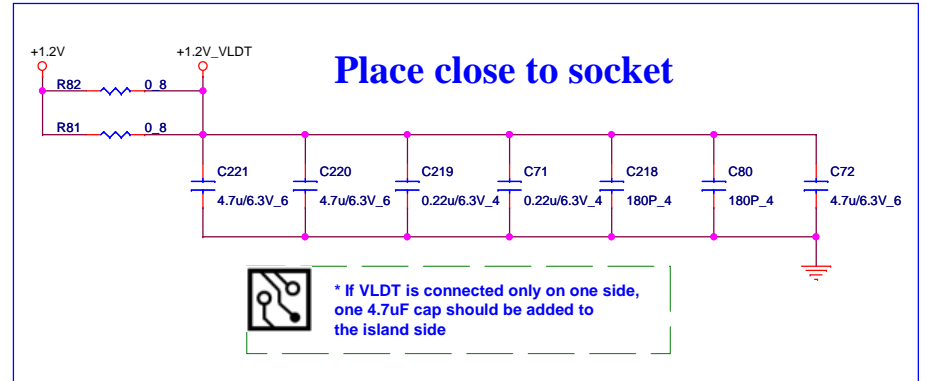
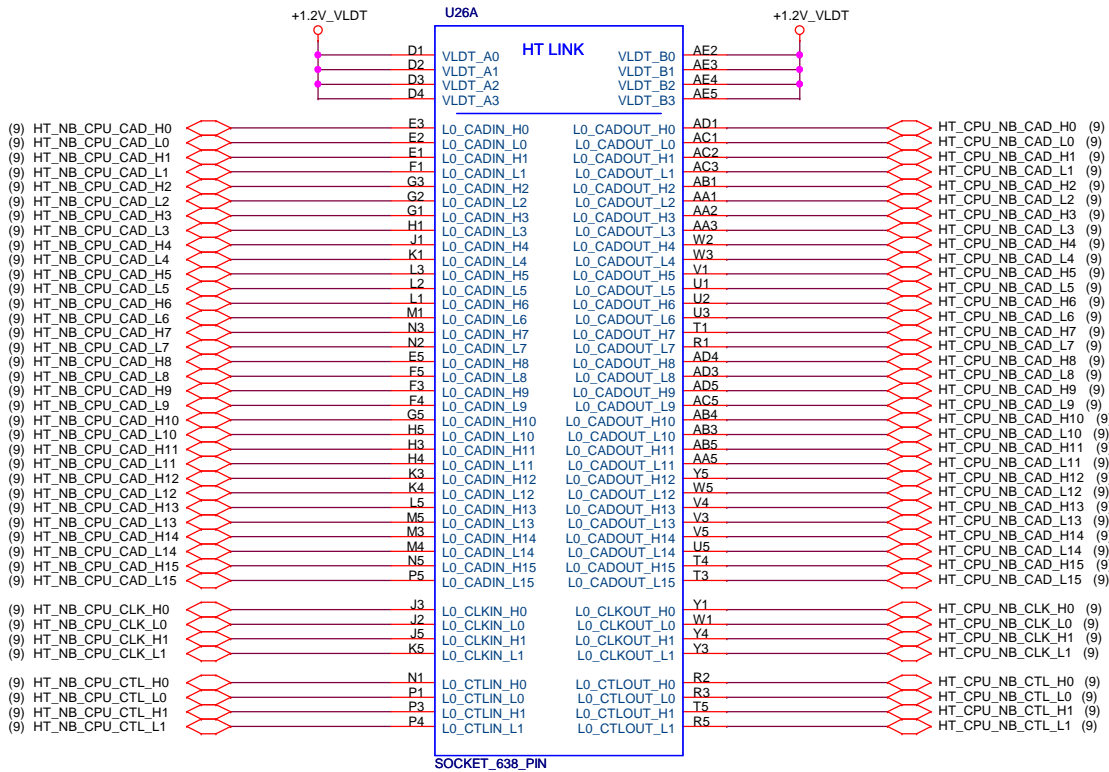
	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

RES CHIP 82.5 1/16W +-1%(0402) -> CS08252FB11
 RES CHIP 130 1/16W +-1%(0402)L.F -> CS11302FB15
 RES CHIP 158 1/16W +-1%(0402) -> CS11582FB00
 RES CHIP 90.9 1/16W +-1%(0402) -> CS09092FB15

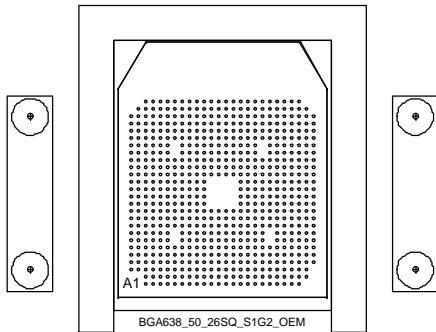
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default





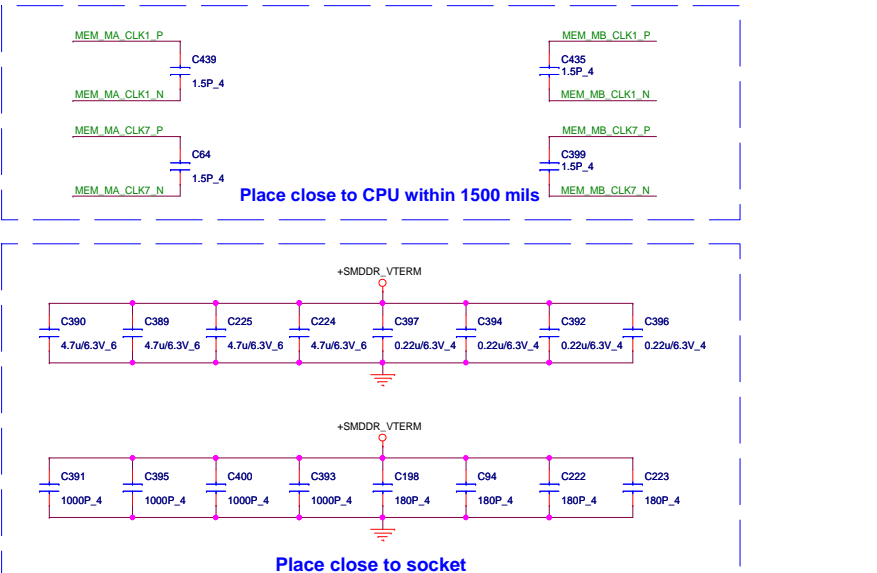
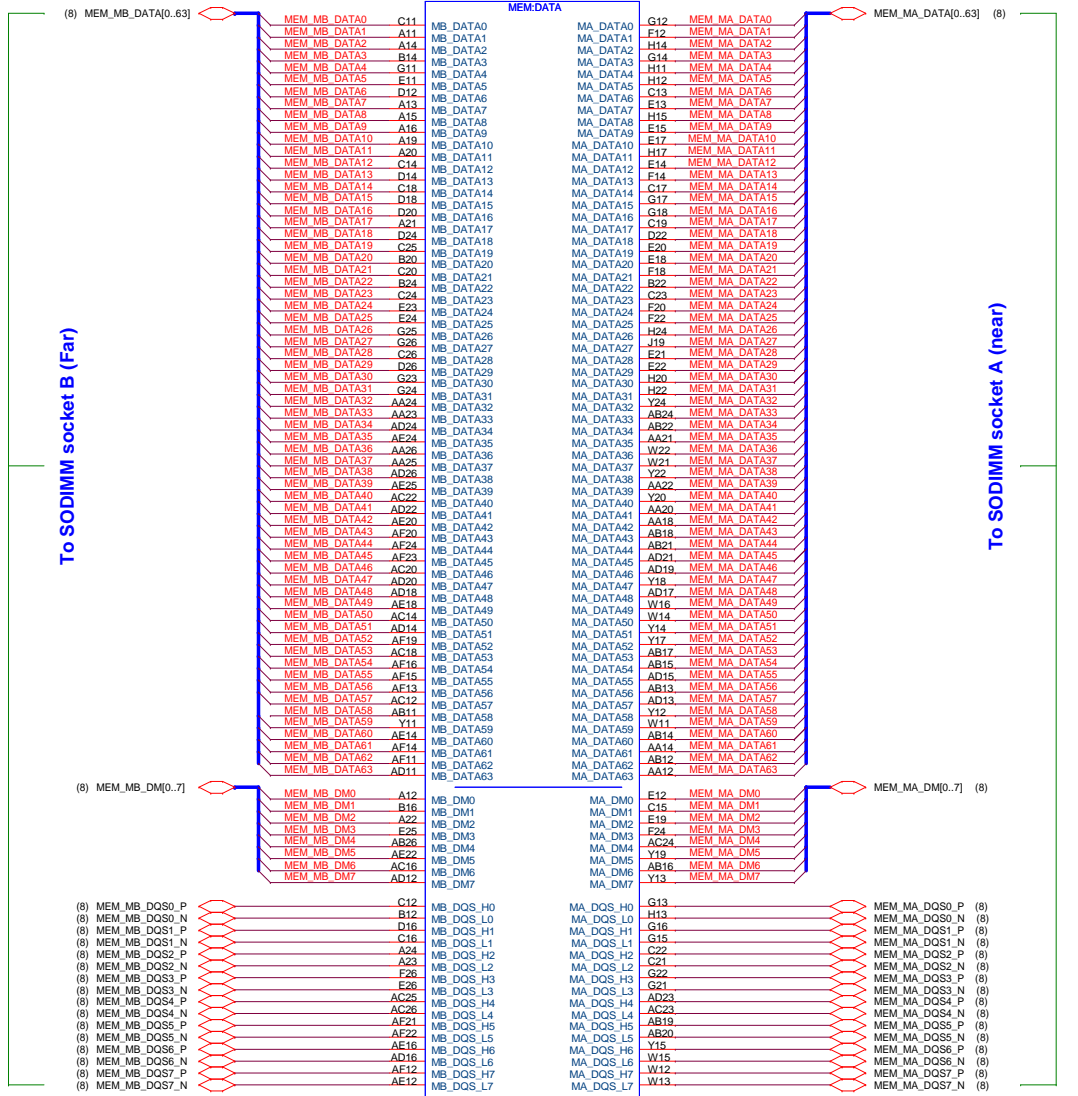
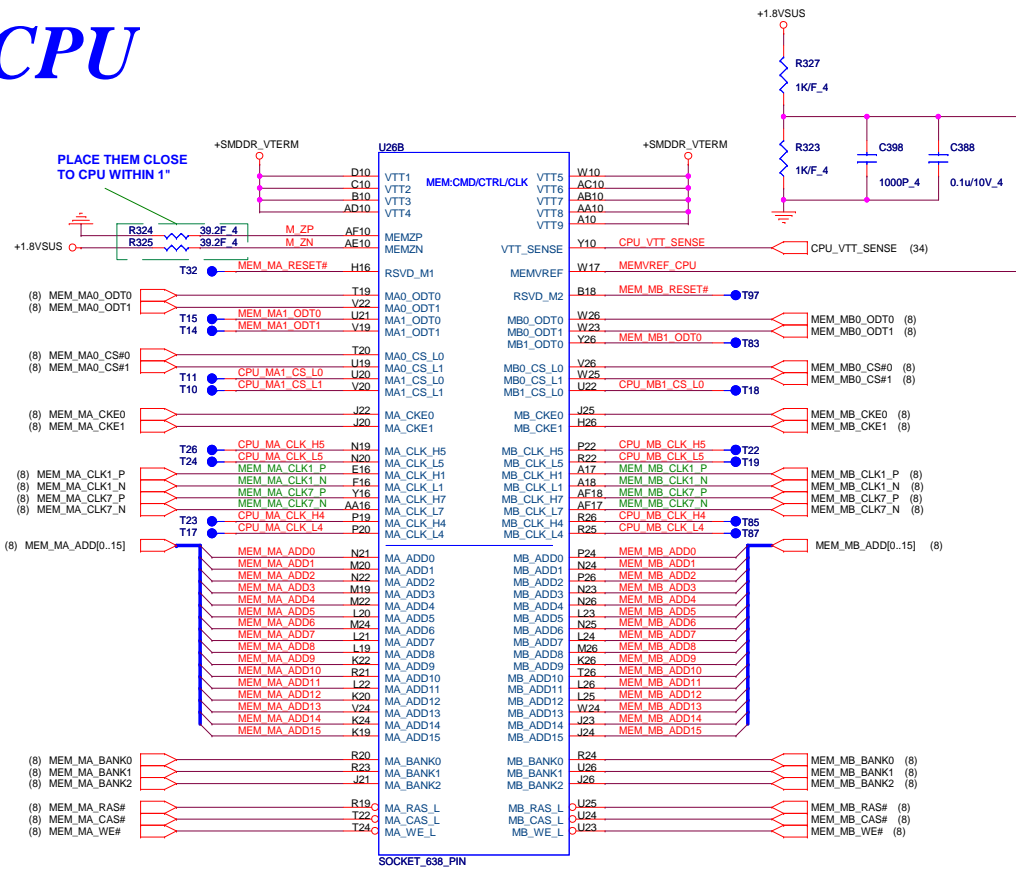
CPU



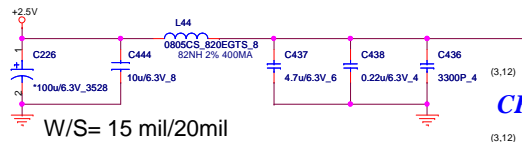
PROJECT : BU2
Quanta Computer Inc.

Size B	Document Number S1G2 HT I/F 1/4	Rev 1A
Date: Thursday, July 24, 2008		Sheet 4 of 35

Processor Memory Interface

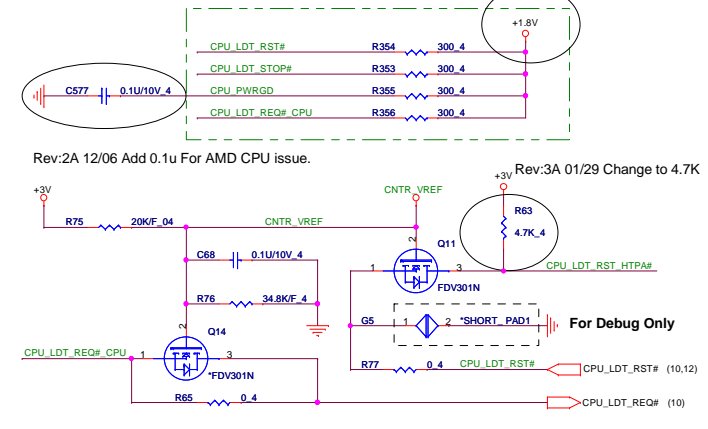


CPU



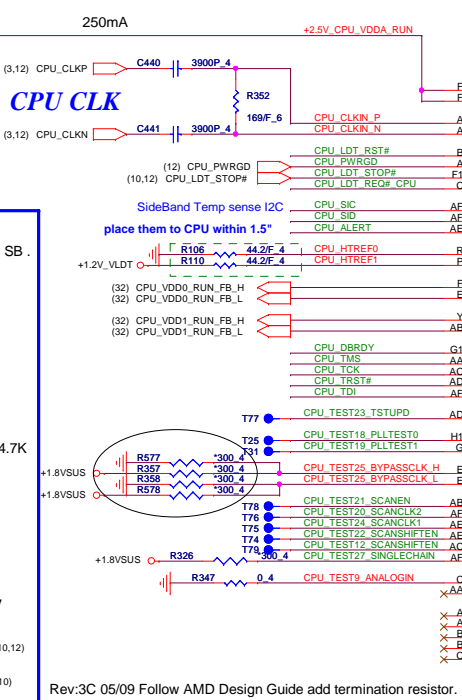
CPU POWER-UP

Rev:3A 01/29 Change to S0 domain save power during S3 since SB.

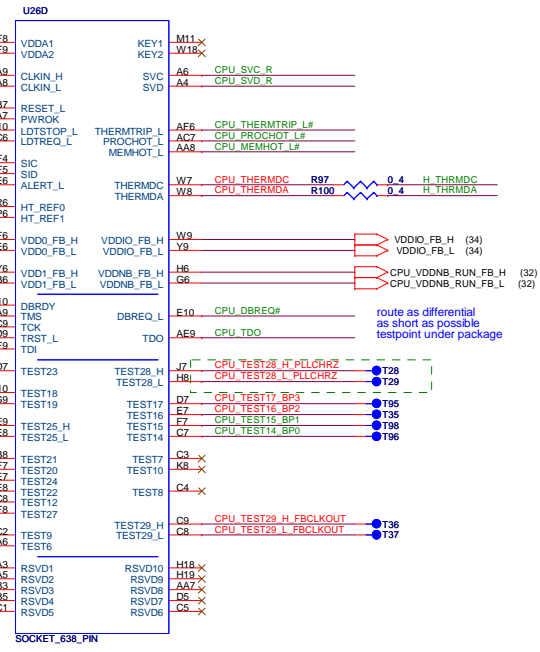


Rev:2A 12/06 Add 0.1u For AMD CPU issue.

Rev:3A 01/29 Change to 4.7K

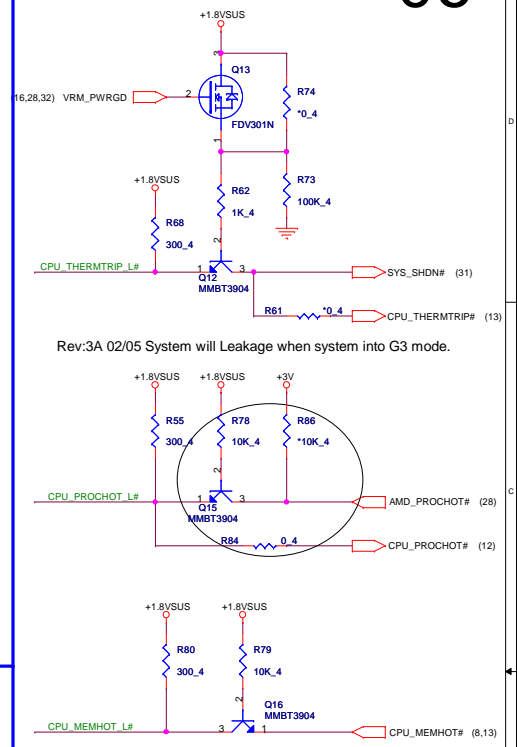


Rev:3C 05/09 Follow AMD Design Guide add termination resistor.

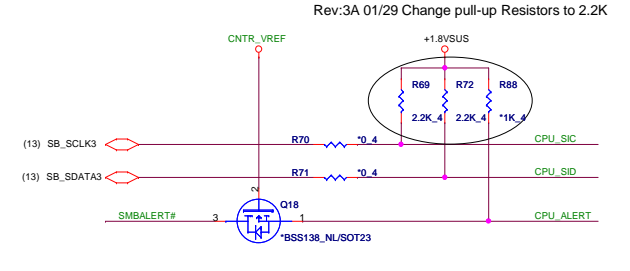
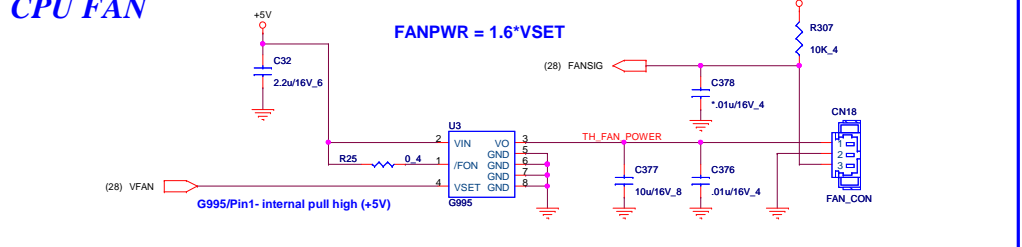


CPU THERM

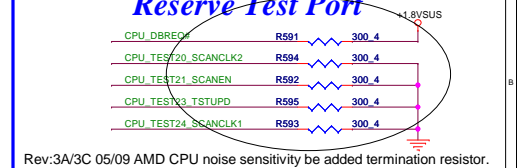
06



CPU FAN

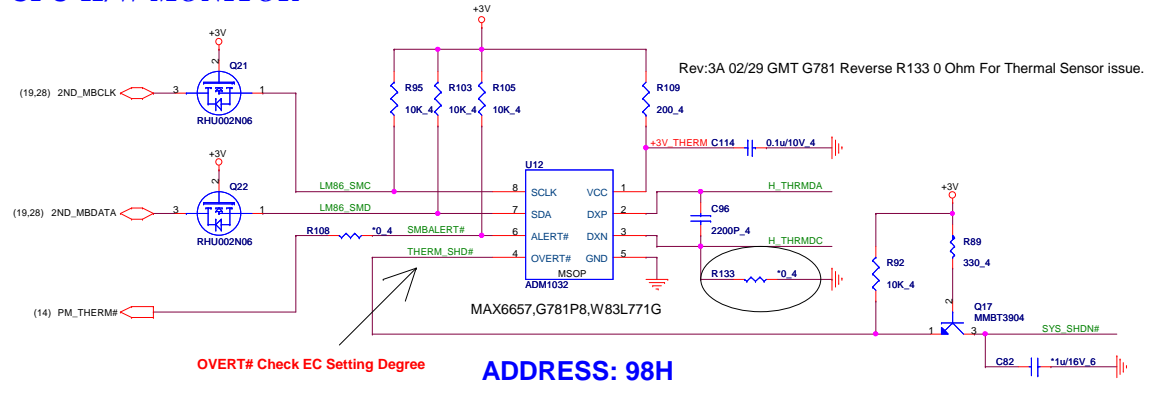


Reserve Test Port

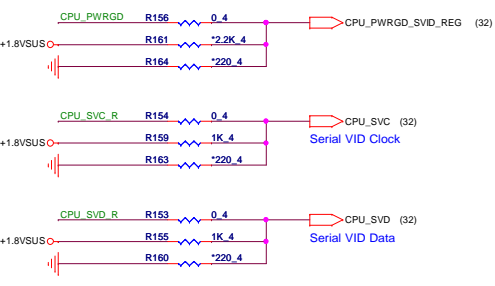


Rev:3A/3C 05/09 AMD CPU noise sensitivity be added termination resistor.

CPU H/W MONITOR



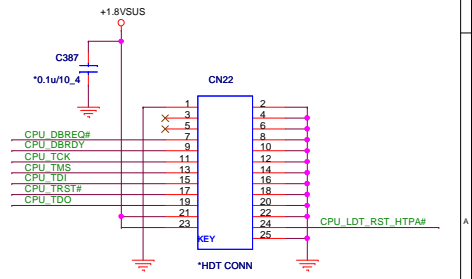
ADDRESS: 98H



VFIX MODE		VID Override Circuit	
SVC	SVD	Voltage Output(CPU Power)	
0	0	1.4V	
0	1	1.2V	
1	0	1.0V	
1	1	0.8V	

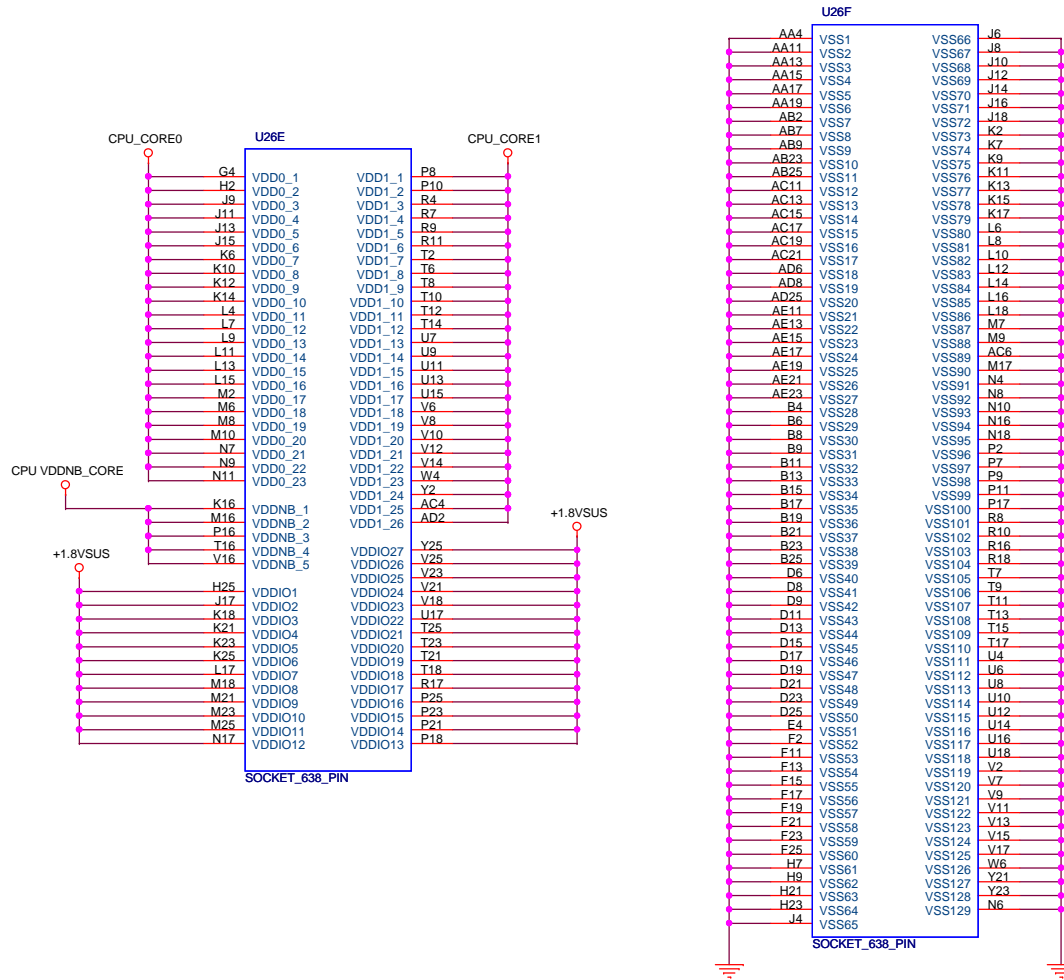
Serial VID

HDT Connector

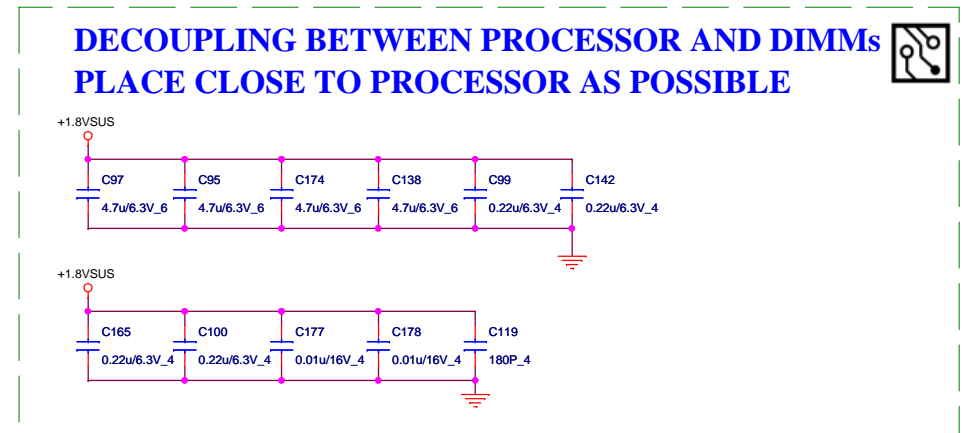
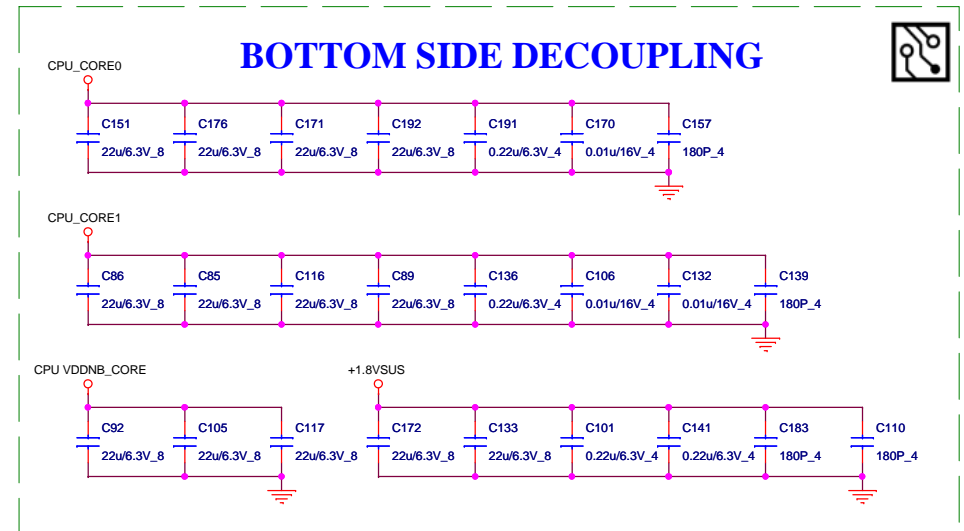


PROJECT : BU2
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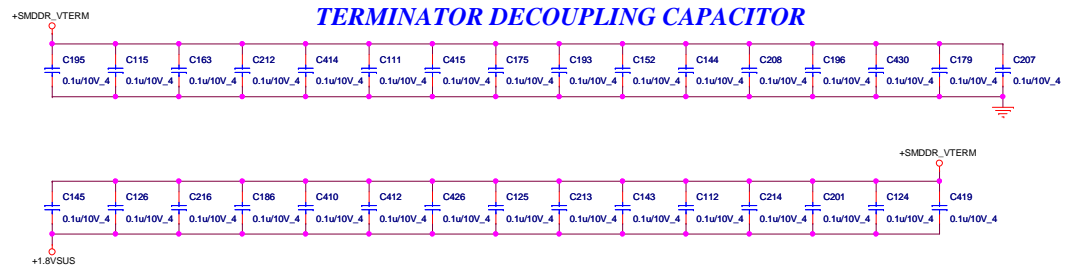
Size Custom	Document Number S1G2 CTRL & DEBUG 3/4	Rev 1A
Date: Thursday, July 24, 2008		Sheet 6 of 35



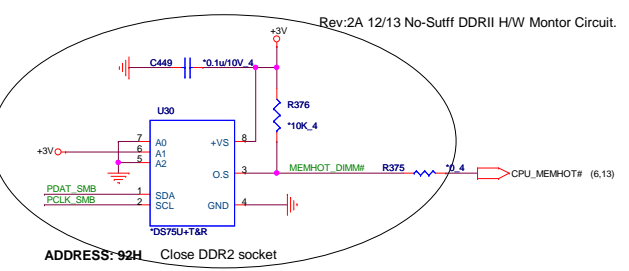
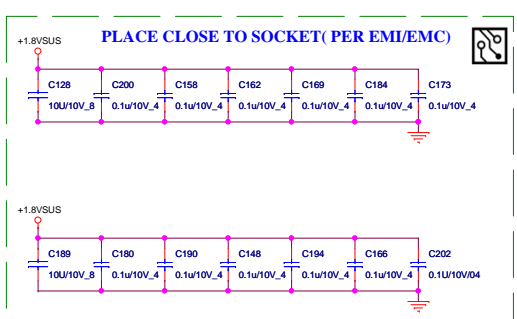
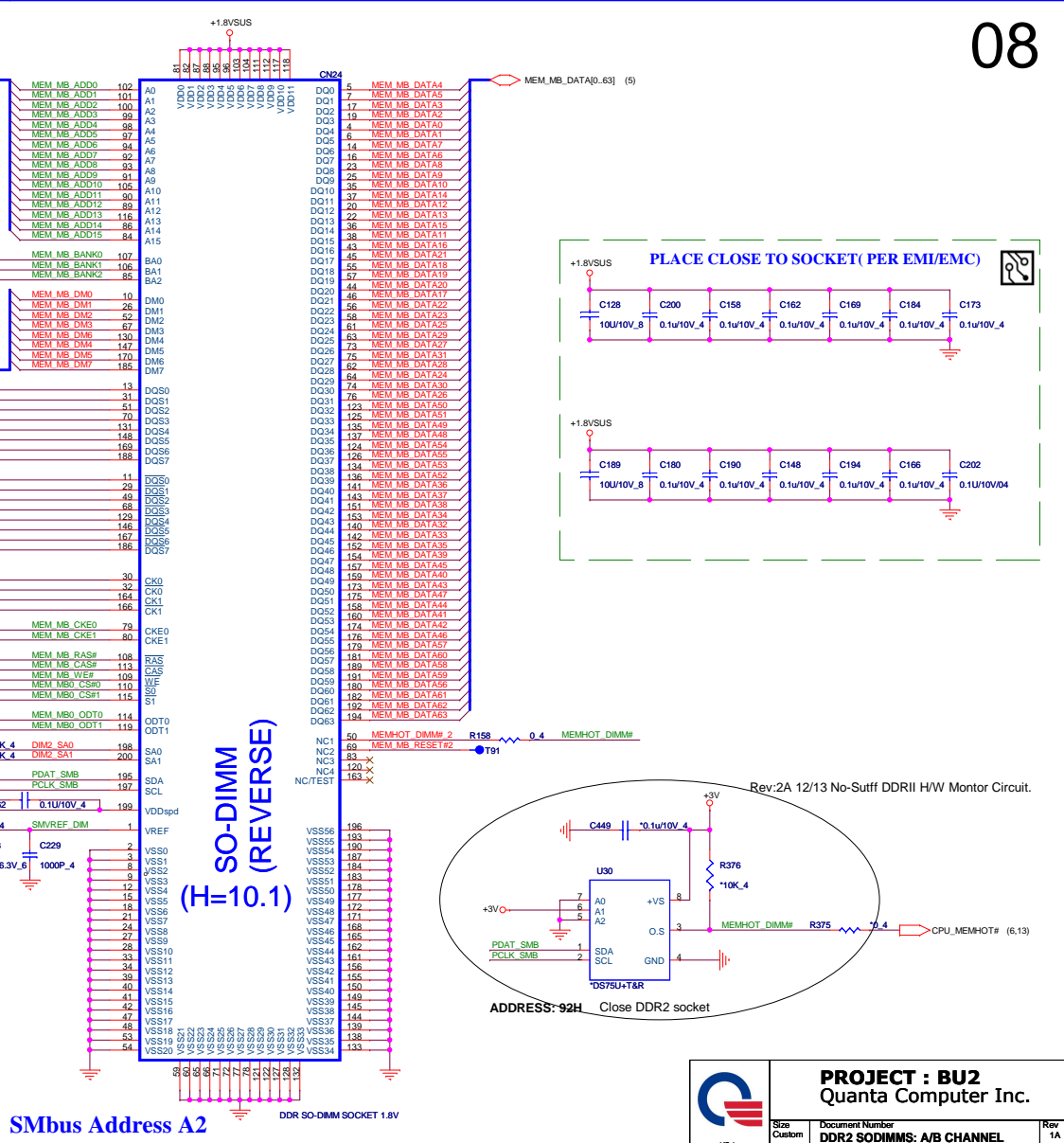
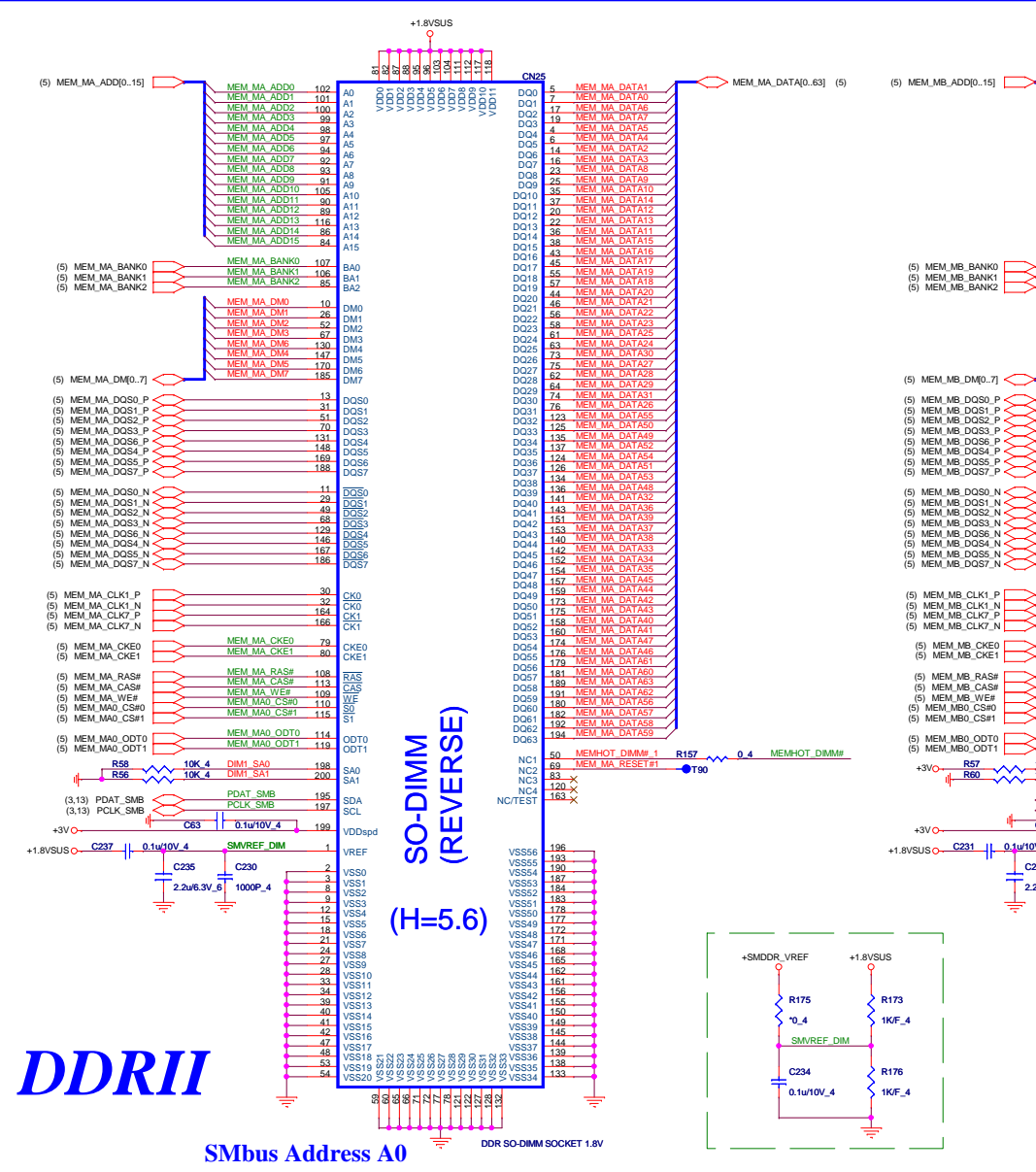
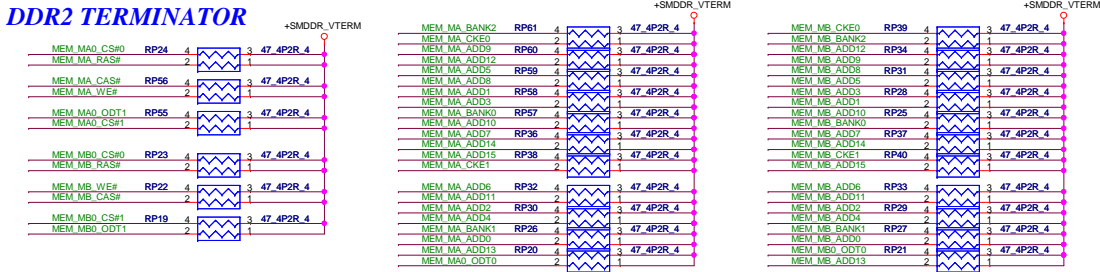
PROCESSOR POWER AND GROUND



TERMINATOR DECOUPLING CAPACITOR



DDR2 TERMINATOR



DDRII

SMBus Address A0

(H=5.6)

SMBus Address A2

(H=10.1)

08

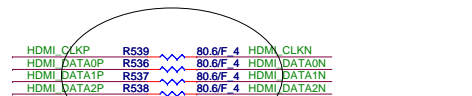
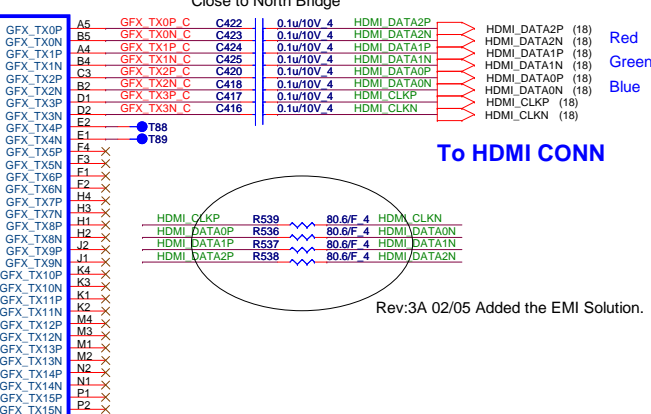
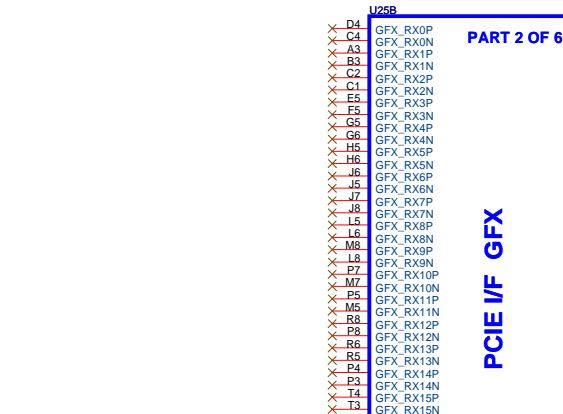
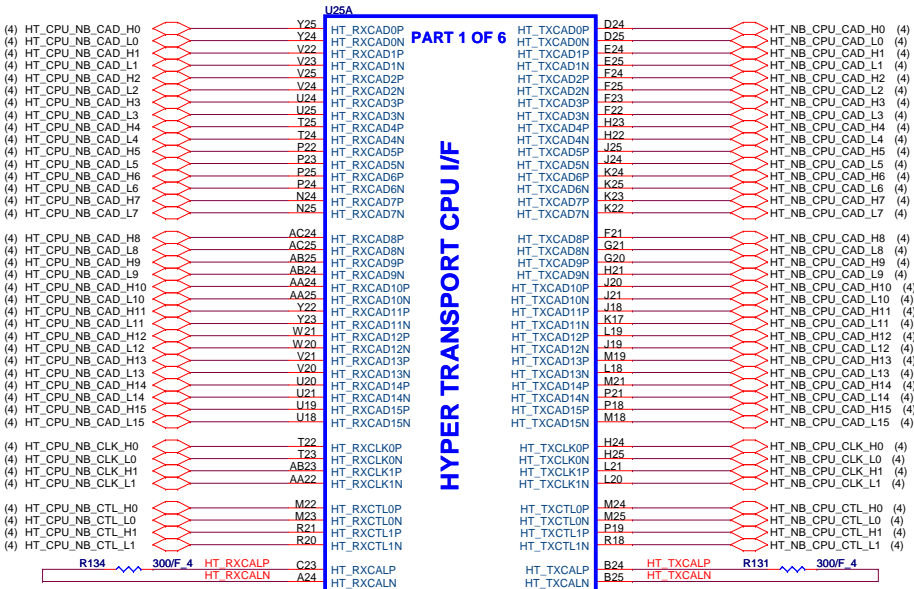
PROJECT : BU2
Quanta Computer Inc.

Size Custom Document Number **DDR2 SODIMMS: A/B CHANNEL** Rev 1A

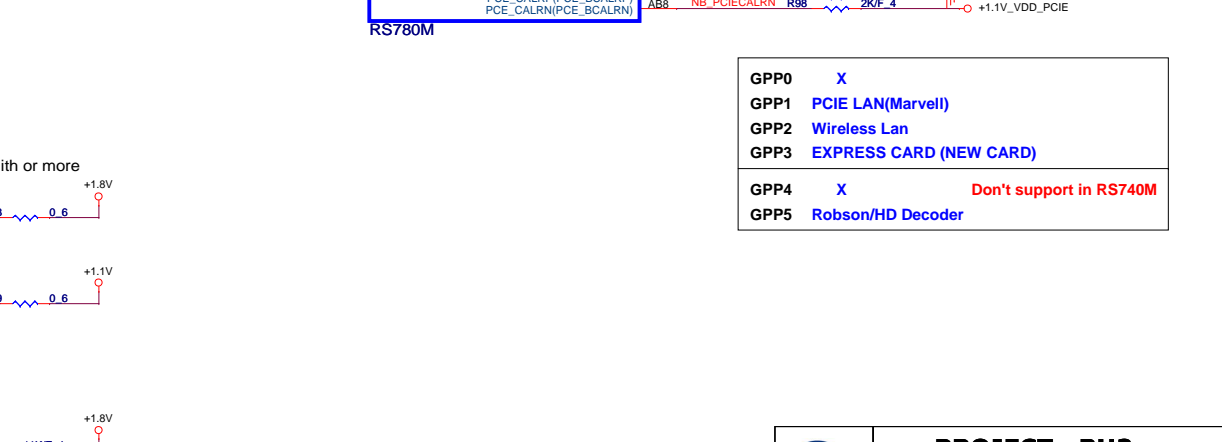
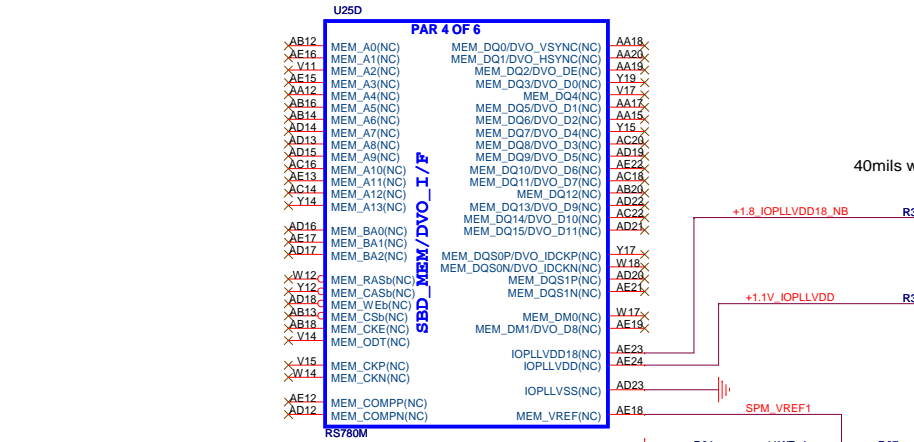
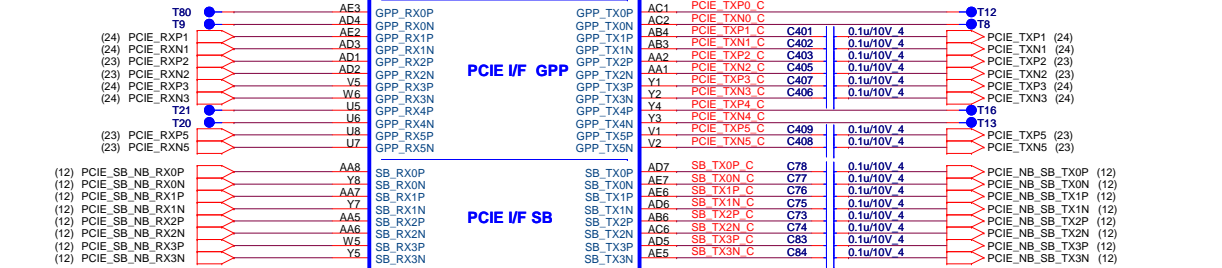
Date: Thursday, July 24, 2008 Sheet 6 of 35

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



Rev:3A 02/05 Added the EMI Solution.



GPP0	X	
GPP1	PCIE LAN(Marvell)	
GPP2	Wireless Lan	
GPP3	EXPRESS CARD (NEW CARD)	
GPP4	X	Don't support in RS740M
GPP5	Robson/HD Decoder	

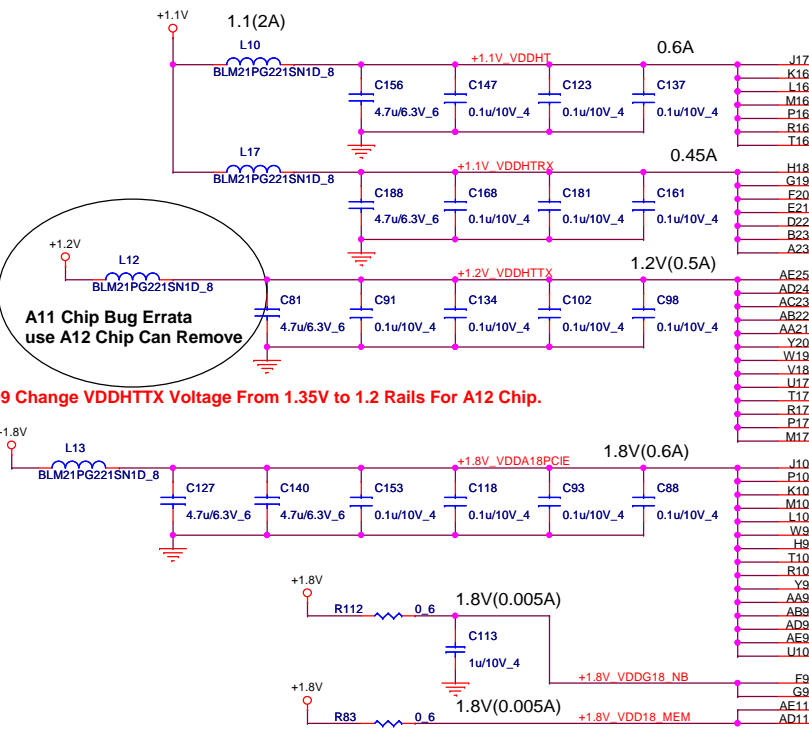
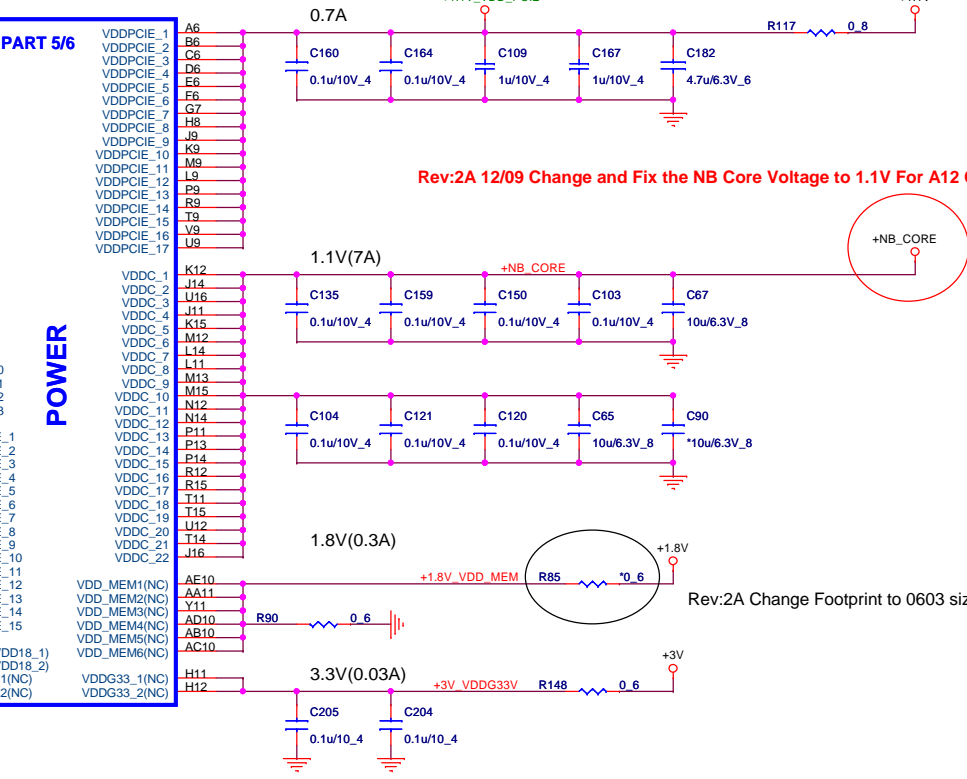
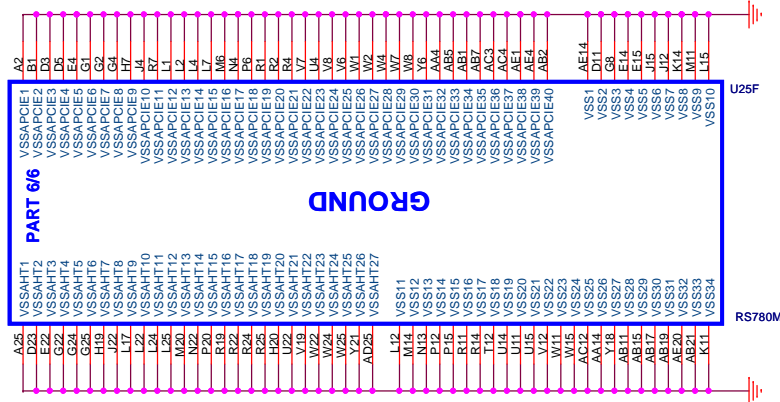
PROJECT : BU2
Quanta Computer Inc.

Size: Custom | Document Number: RS740/RS780-HT LINK/PCIE I/F 1/4 | Rev: 1A

Date: Thursday, July 24, 2008 | Sheet 9 of 35

RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC



A11 Chip Bug Errata use A12 Chip Can Remove

Rev:2A 12/09 Change VDDHTTX Voltage From 1.35V to 1.2 Rails For A12 Chip.

Rev:2A 12/09 Change and Fix the NB Core Voltage to 1.1V For A12 Chip.

Rev:2A Change Footprint to 0603 size

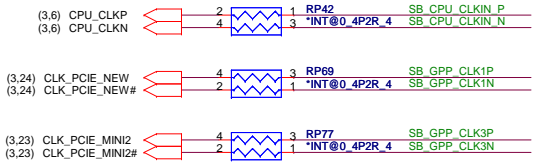
RS780



PROJECT : BU2
Quanta Computer Inc.

Size Custom	Document Number RS740/RS780-POWER5/5	Rev 1A
Date: Thursday, April 10, 2008	Sheet 11	of 35

FOR INTERNAL CLOCK



Place close to CLK GEN

1. PCIE Reference Clk(Ext Clk Gen)
2. A-Link Clk to North Bridge(Int Clk Gen)

From Clk Gen Input

To NB A-Link CLK

For North Bridge

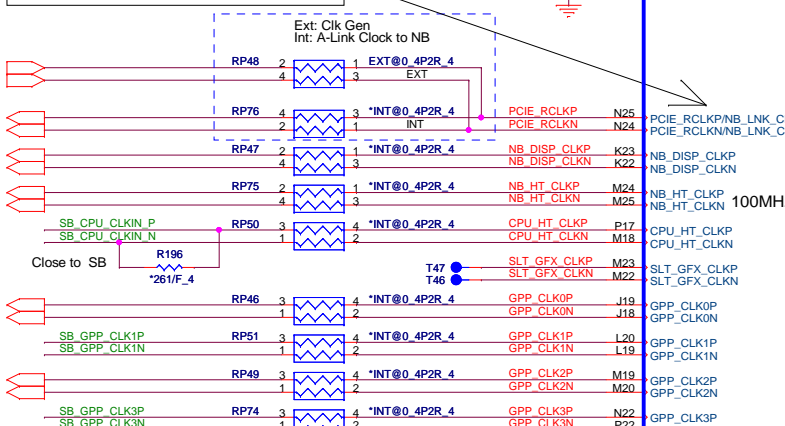
For North Bridge

For CPU Host Clk

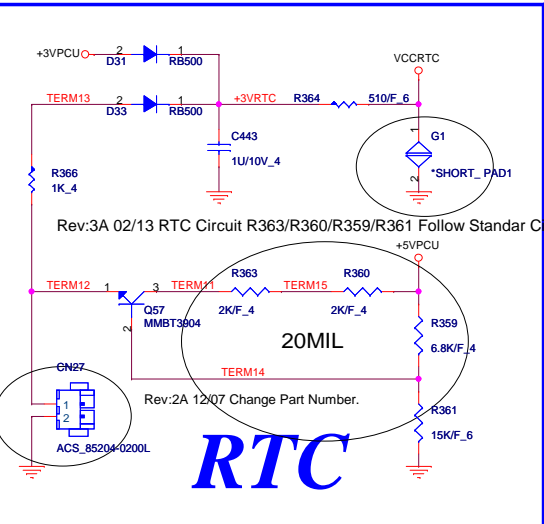
To Marvell Lan

To New Card

To Mini Card 1,2

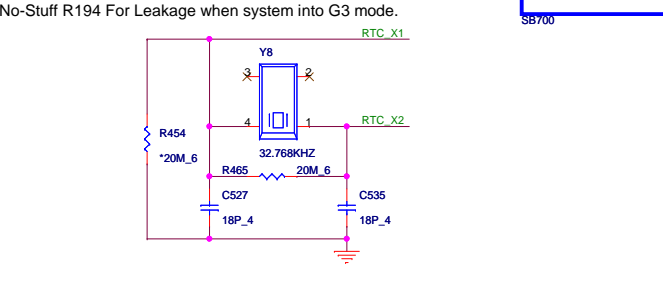
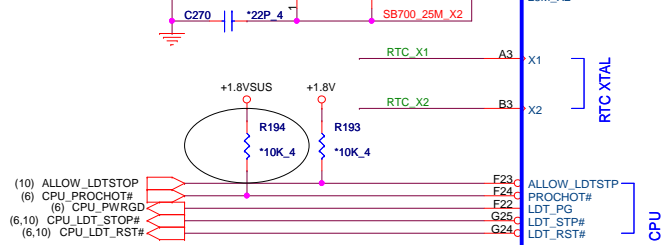


Rev:3B 04/02 As the same location Name(G1) For Toshiba Service Team Request.

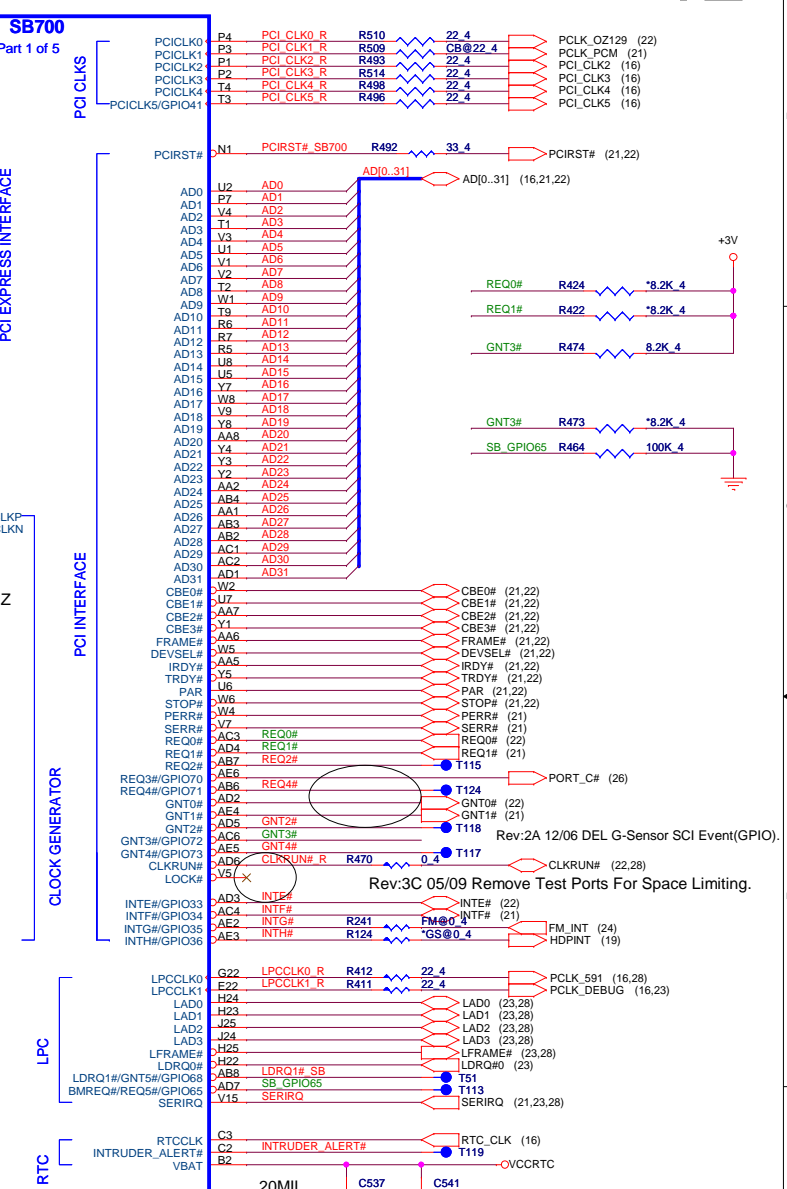
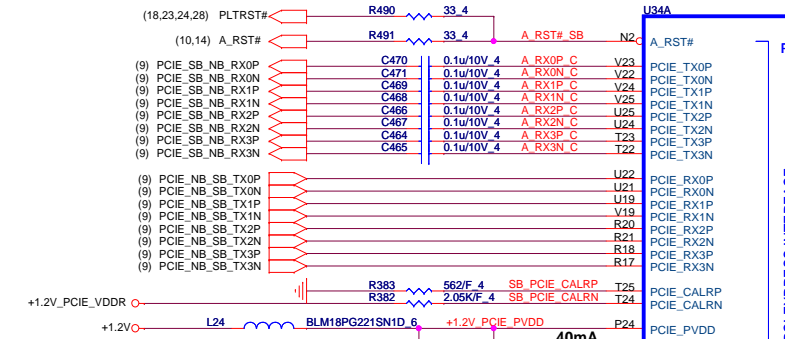


RTC

Install for Int Clk Gen



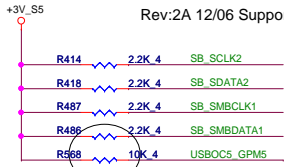
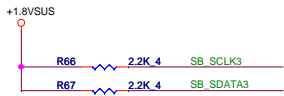
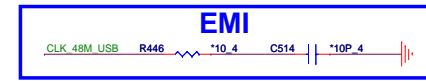
AC COUPLING CAPS CLOSE TO SB700



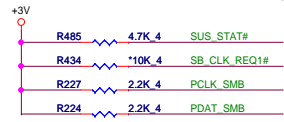
PROJECT : BU2
Quanta Computer Inc.

Size Custom
Document Number **SB700-PCIE/PCU/LPC 1/4**
Date: Thursday, July 24, 2008 | Sheet 12 of 35

Rev 1A

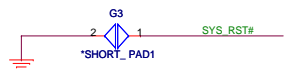


Rev:3B 04/07 USB Overcurrent 5 Pull-up 10K For Open Drain.



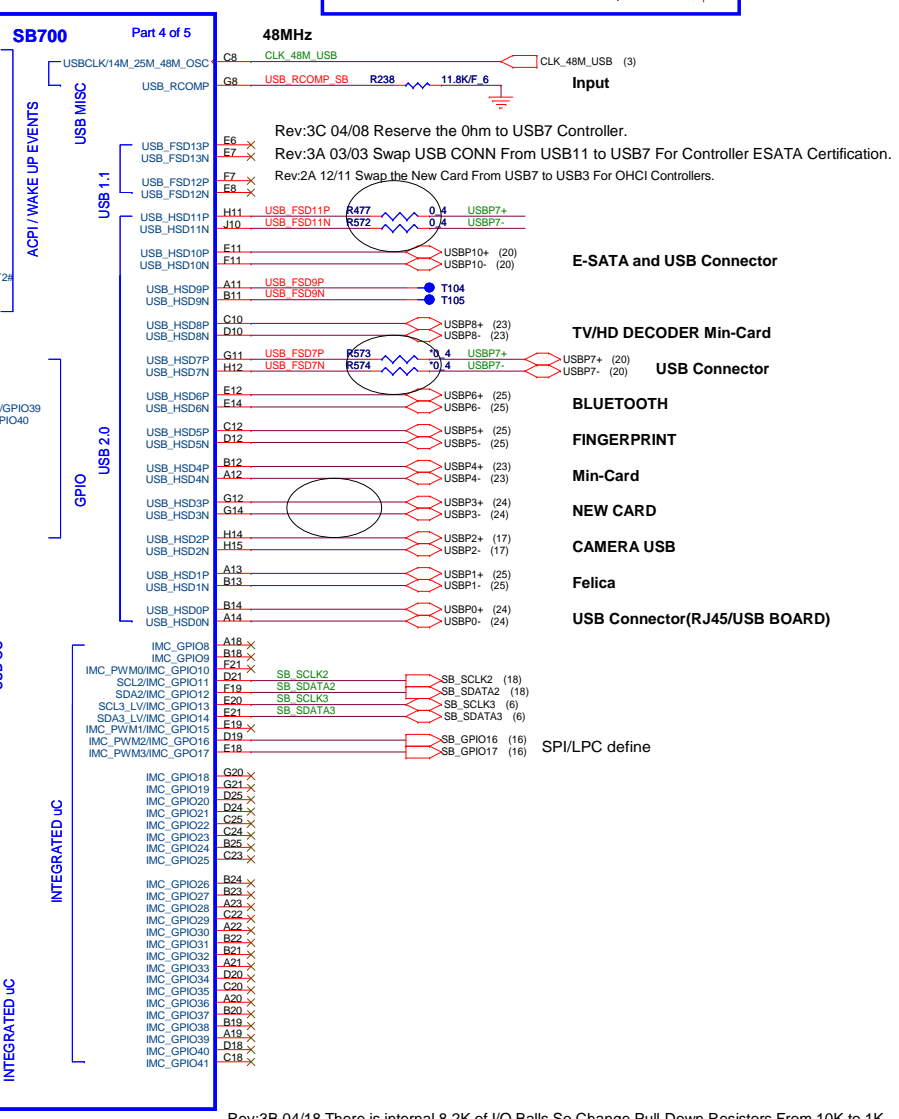
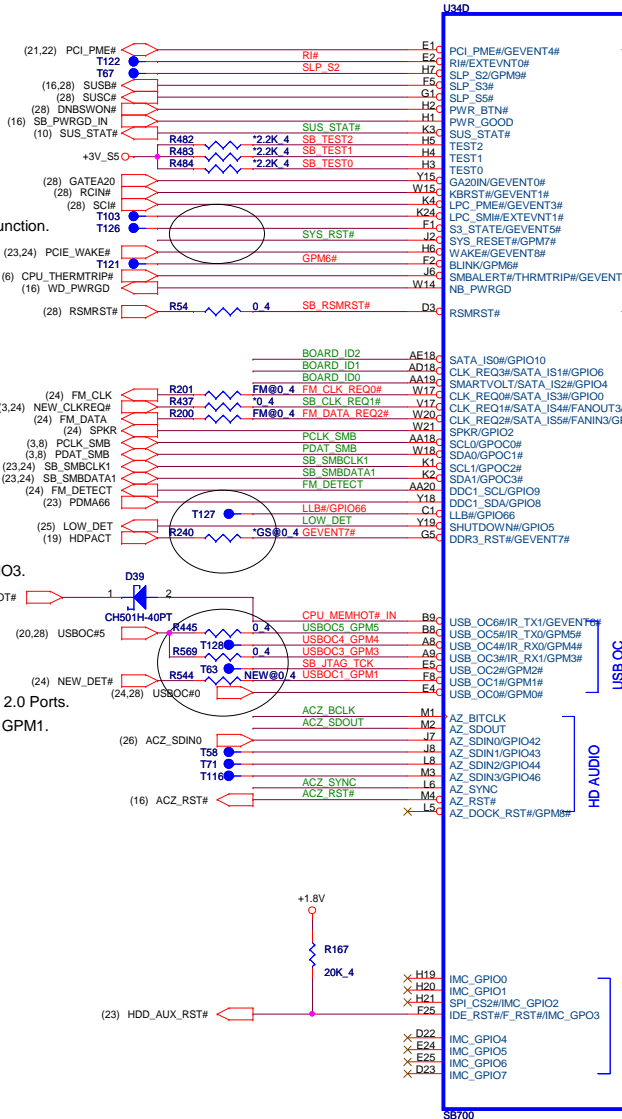
Rev:2A 12/06 DEL G-Sensor SCI Event(GPIO).

Rev:3A 02/05 Move Board ID4 Pin Name From GPIO66 to GPIO3.



Rev:3B 04/07 Added the USB Overcurrent 3 to Support USB 2.0 Ports.

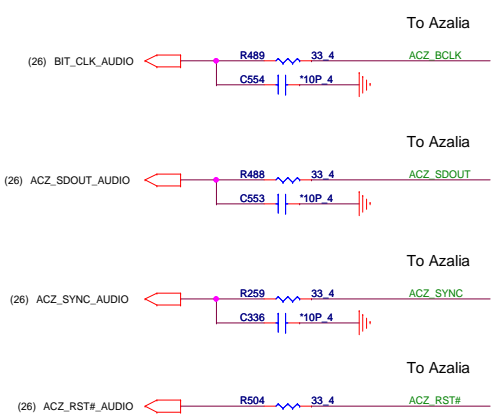
Rev:3A 02/05 Move Hot Plug Pin Name From EVENT5# to GPM1#.



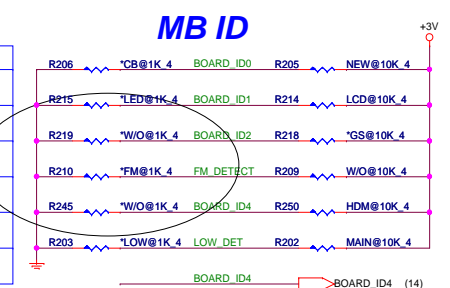
Rev:3C 04/08 Reserve the 0hm to USB7 Controller.
 Rev:3A 03/03 Swap USB CONN From USB11 to USB7 For Controller ESATA Certification.
 Rev:2A 12/11 Swap the New Card From USB7 to USB3 For OHCI Controllers.

- E-SATA and USB Connector
- TV/HD DECODER Min-Card
- USB Connector
- BLUETOOTH
- FINGERPRINT
- Min-Card
- NEW CARD
- CAMERA USB
- Felica
- USB Connector(RJ45/USB BOARD)

HD Audio Interface



BOARD_ID	BOARD_ID0	BOARD_ID1	BOARD_ID2	FM_DETECT	BOARD_ID4	LOW_DET
W/ New Crad W/ Crad Bus	H	L				
W/ CCFL Panel W/ LED Panel		H	L			
W/ G-Sensor W/O G-Sensor			H	L		
W/O FM W/FM				H	L	
W/ HDMI W/O HDMI					H	L
Main Stream Low Cost						H



Rev:3B 04/18 There is internal 8.2K of I/O Balls So Change Pull-Down Resistors From 10K to 1K.

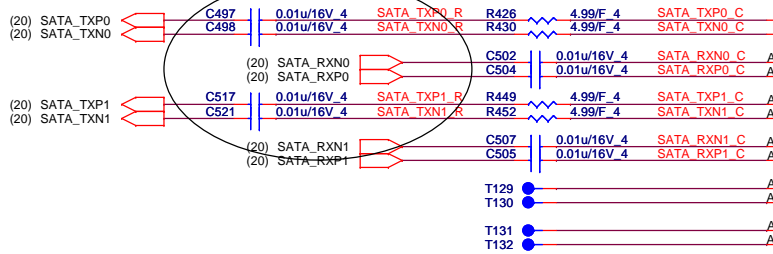
PROJECT : BU2
Quanta Computer Inc.

Size Custom	Document Number	Rev
	SB700-ACPI/GPIO/USB 2/4	1A
Date: Thursday, July 24, 2008		Sheet 13 of 35

SB700

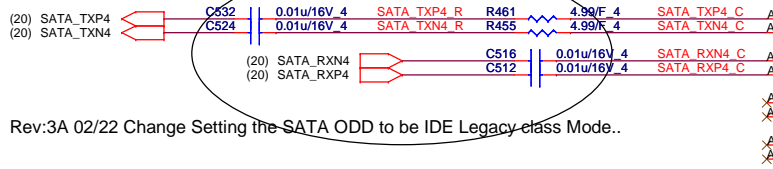
PLACE SATA AC COUPLING CAPS CLOSE TO SB700

SATA HDD



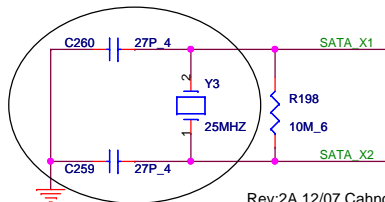
Rev:3B 04/18 Change HDD Control From Channel/2 to Channel/0 For Spin Down Issue.

SATA ODD

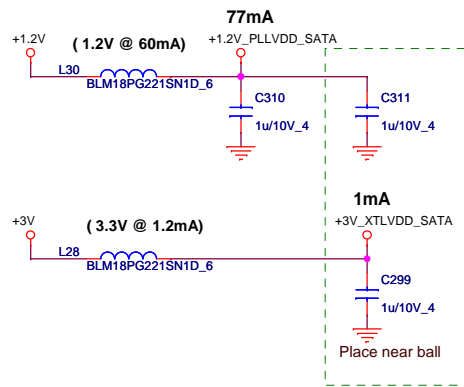


Rev:3A 02/22 Change Setting the SATA ODD to be IDE Legacy class Mode..

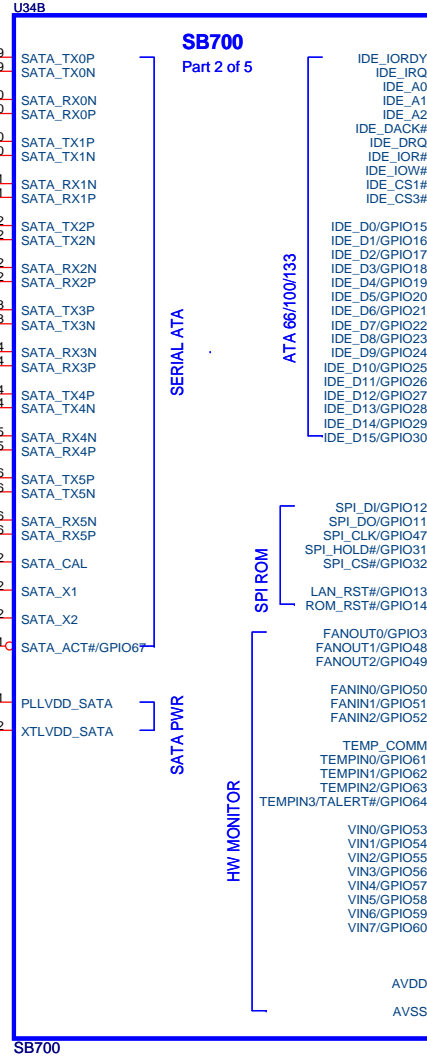
NOTE:
 R635 IS 1K 1% FOR 25MHZ XTAL, 4.99K 1% FOR 100MHZ INTERNAL CLOCK



Rev:2A 12/07 Change C259/C260 Load Capacitance For Matching Crystal.



Place near ball

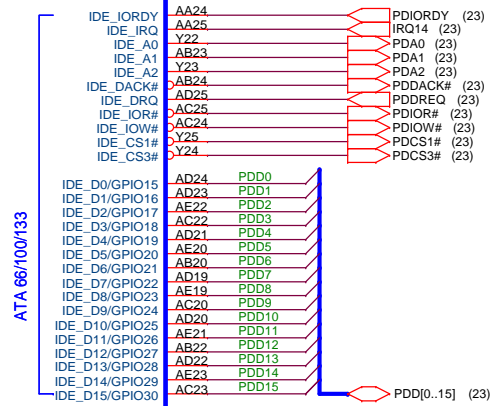


SB700 Part 2 of 5

SERIAL ATA

SATA PWR

HW MONITOR



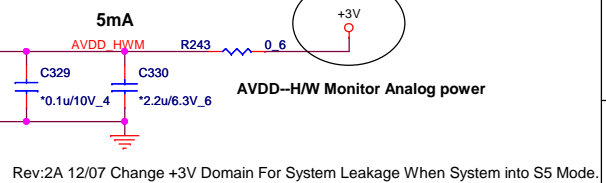
SPI ROM



Rev:3C 04/08 Reserve the Board ID For USB Controller.
Rev:3A 02/05 Added the Board ID4 to GPIO3.

Rev:3C 05/09 Remove Test Ports For Space Limiting.

Rev:3C 05/09 Remove Test Ports For Space Limiting.



Rev:2A 12/07 Change +3V Domain For System Leakage When System into S5 Mode.

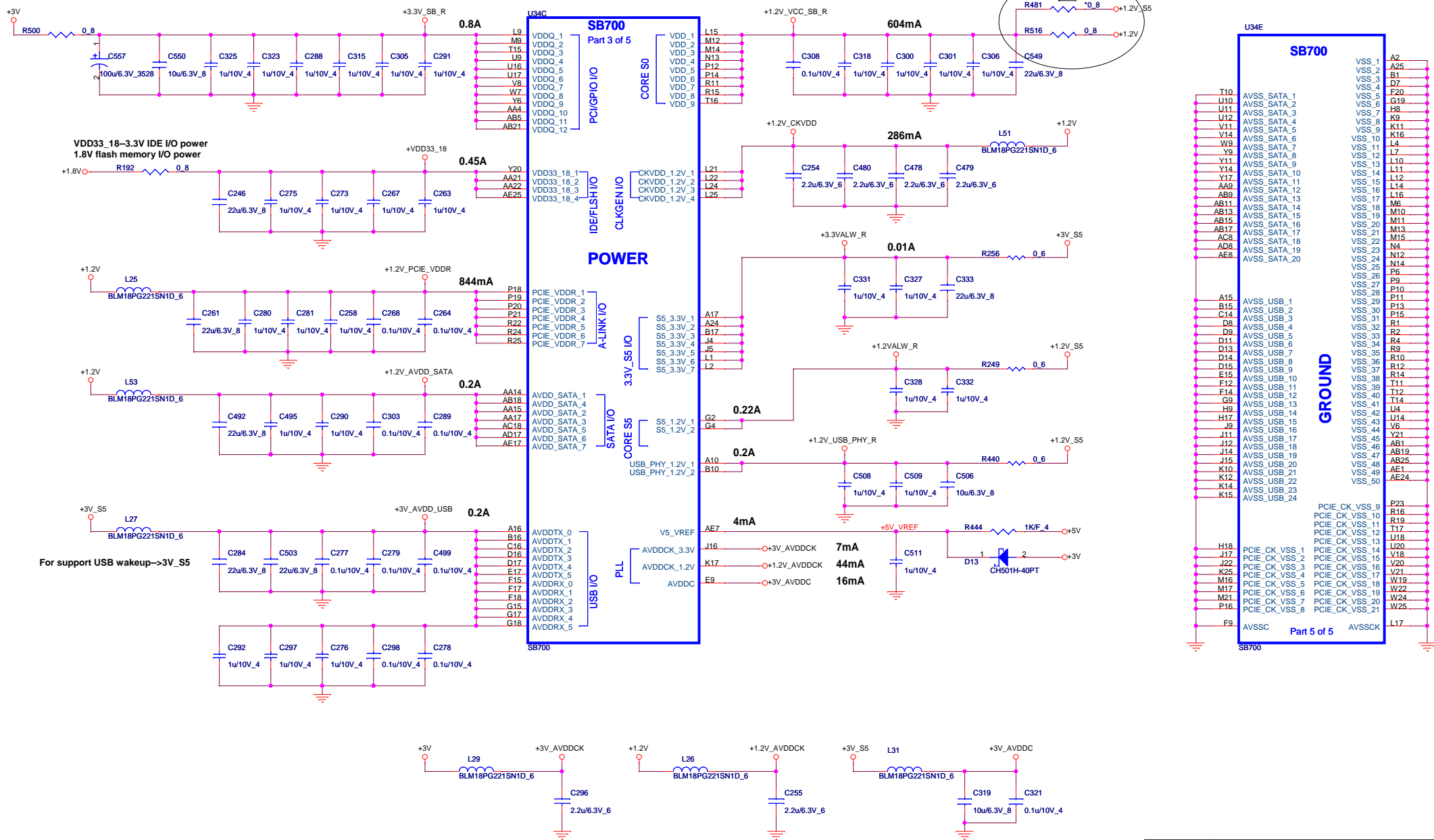
PROJECT : BU2
Quanta Computer Inc.

Size Custom	Document Number SB700-ACPI/GPIO/USB 2/4	Rev 1A
Date: Thursday, July 24, 2008		Sheet 14 of 35

Rev:2A 12/10 The VDD Power Pin to be connected to S0_1.2V Power For A12 Chip.

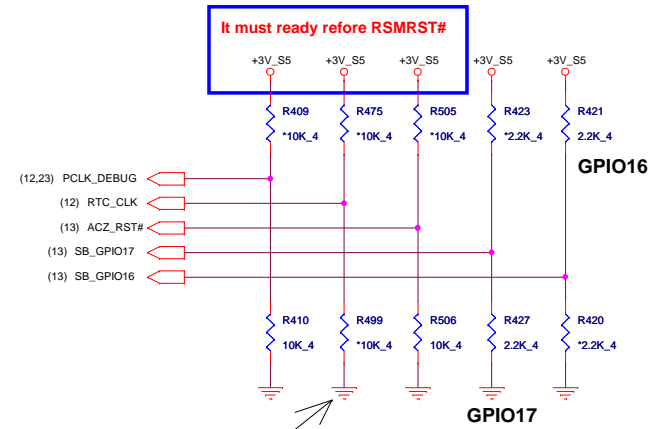
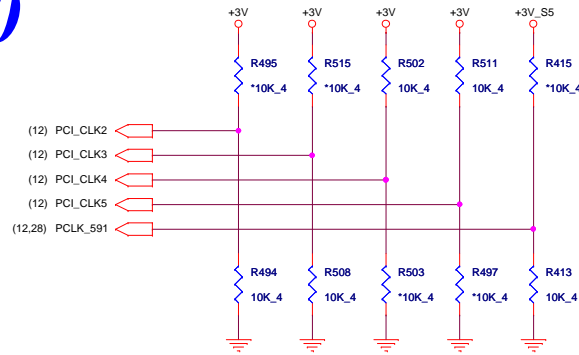
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

A11 Chip Bug use A12 Chip Can Remove



PROJECT : BU2
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	SB700-PWR/DECOUPLING 4/4	
Date: Friday, May 09, 2008	Sheet 15 of 35	



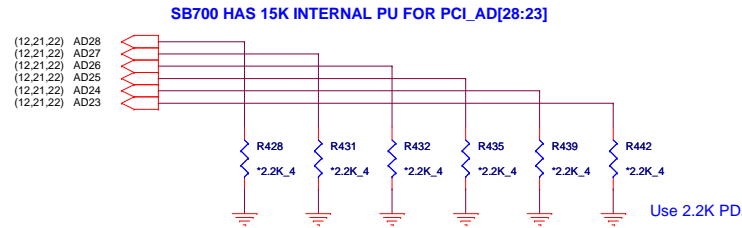
NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

REQUIRED STRAPS

PULL HIGH	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0
	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT

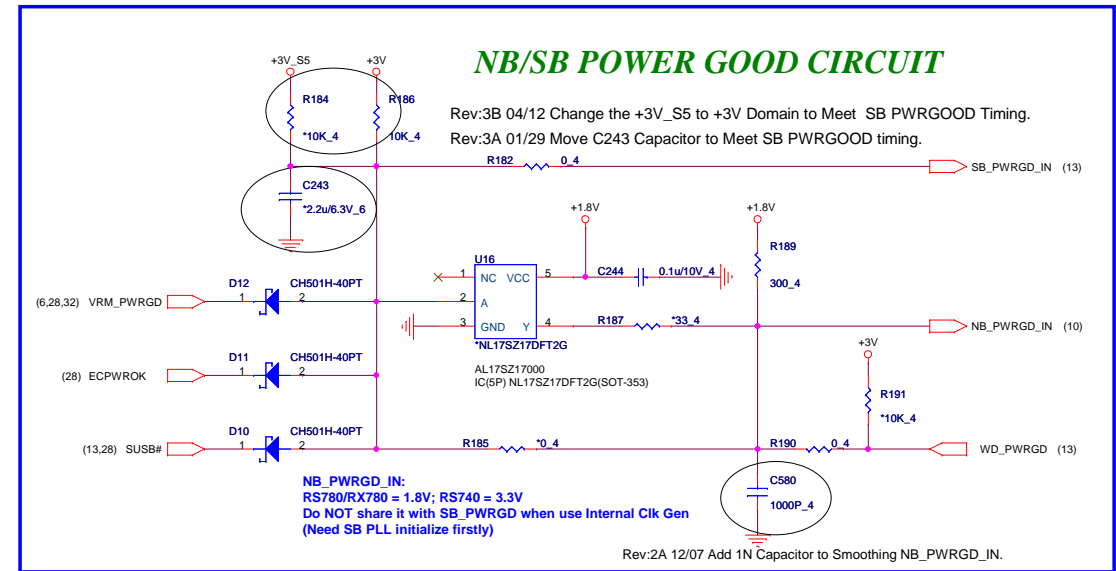
PULL HIGH	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17	GP16
	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED		ROM TYPE: H, H = Reserved H, L = SPI ROM
PULL LOW	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L, H = LPC ROM L, L = FWB ROM DEFAULT

DEBUG STRAPS

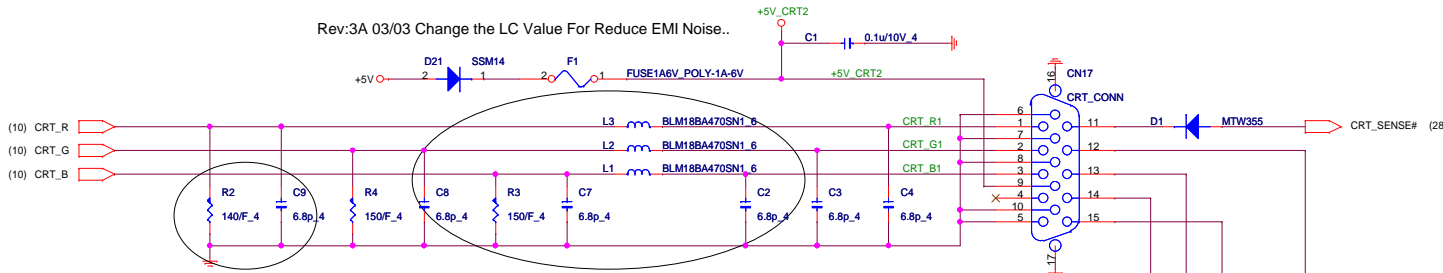


REQUIRED STRAPS

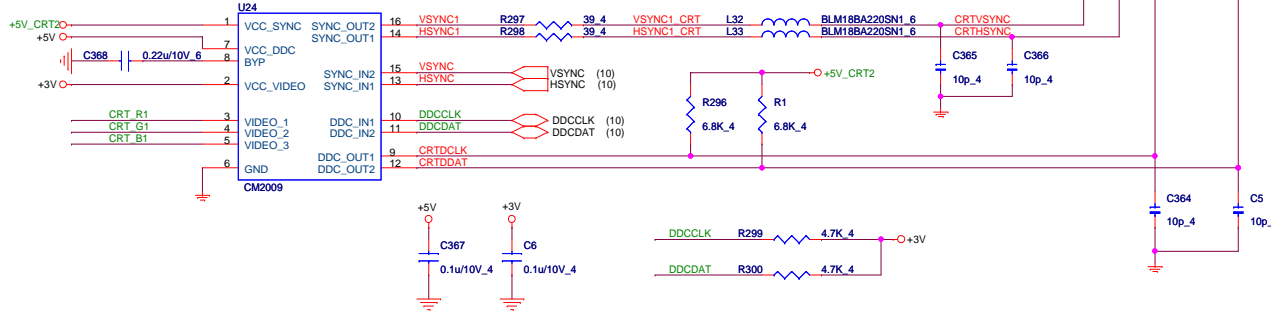
PULL HIGH	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



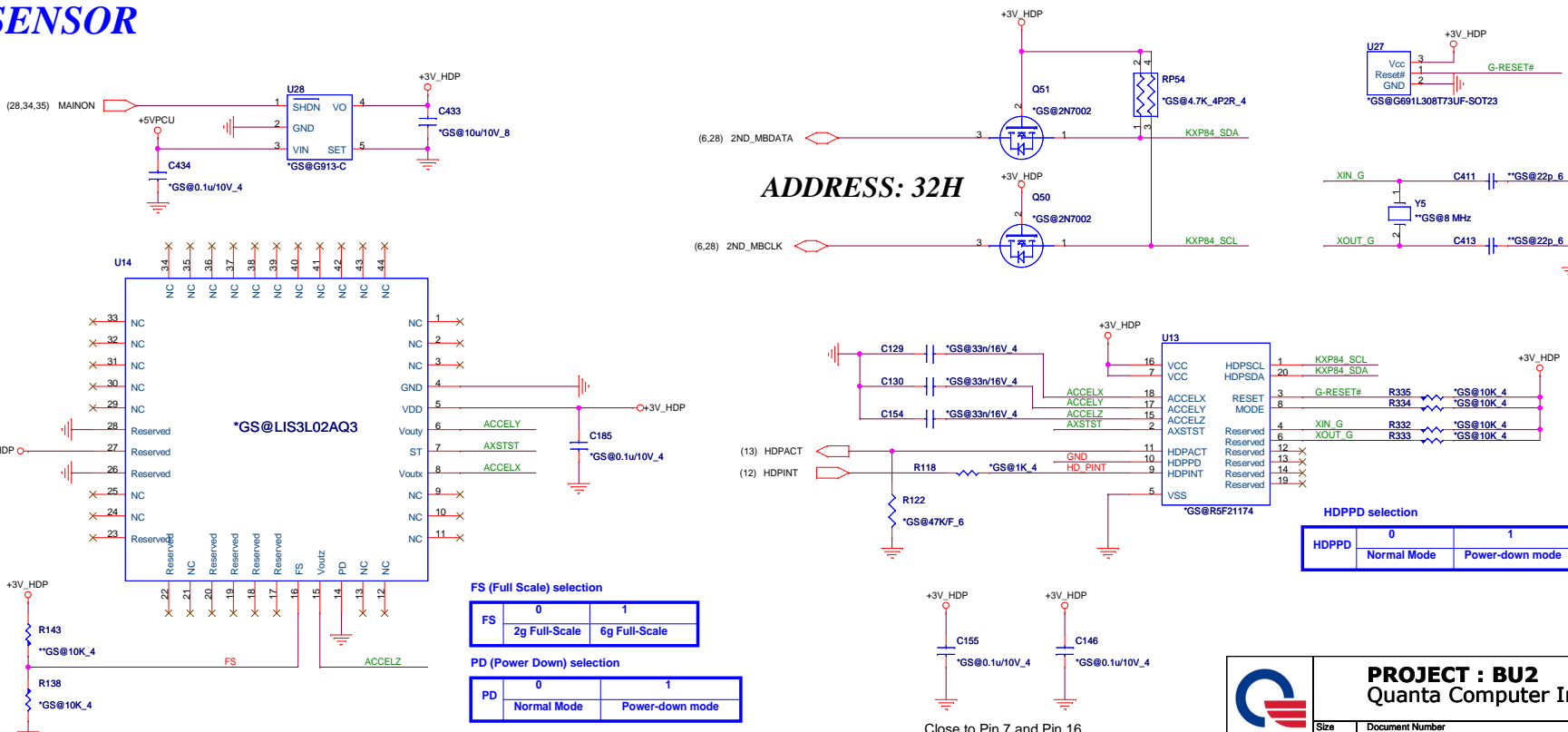
Rev:3A 03/03 Change the LC Value For Reduce EMI Noise..



Rev:3A 02/13 Follow A13 silicon Change R2 From 150 To 140ohm For Unbalanced power bus IR drop..



G-SENSOR



HDDPP selection

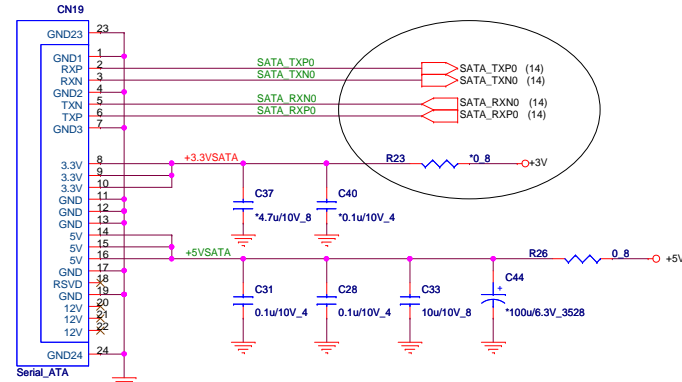
HDDPP	0	1
	Normal Mode	Power-down mode

PROJECT : BU2
Quanta Computer Inc.

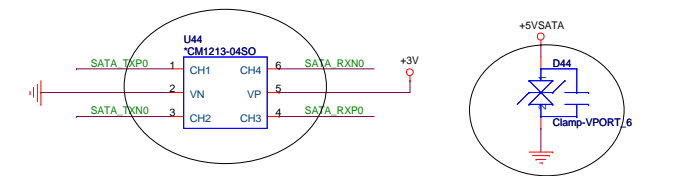
Size Custom	Document Number	Rev
	CRT & G-SENSOR(LIS3L02A)	1A
Date: Thursday, July 24, 2008		Sheet 19 of 35

Close to Pin 7 and Pin 16

SATA HDD

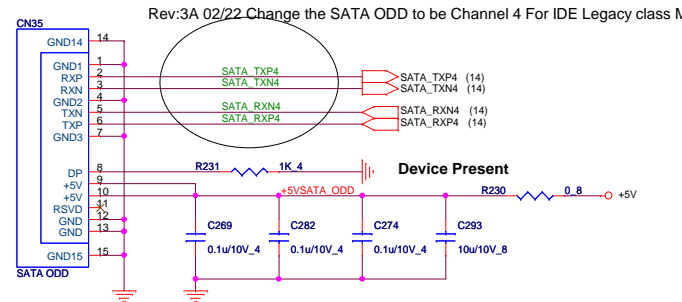


Rev:3B 04/18 Change HDD Control From Channel/2 to Channel/0 For Spin Down Issue.

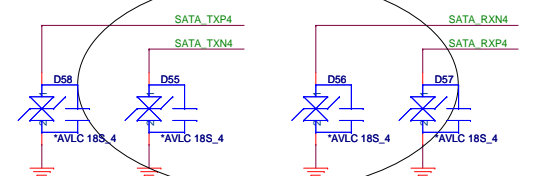


Rev:3B 04/18 Remove D51/D52/D53/D54 Varistor And Change to U44 CM1213-04SO ESD Protection Arrays.

SATA ODD

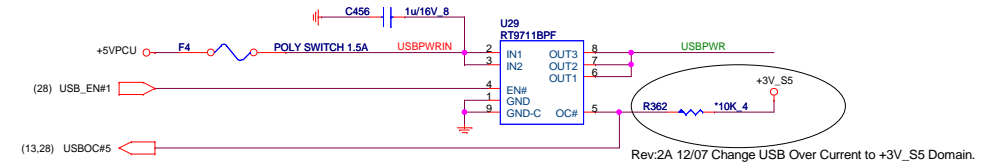


Rev:3A 02/22 Change the SATA ODD to be Channel 4 For IDE Legacy class Mode..

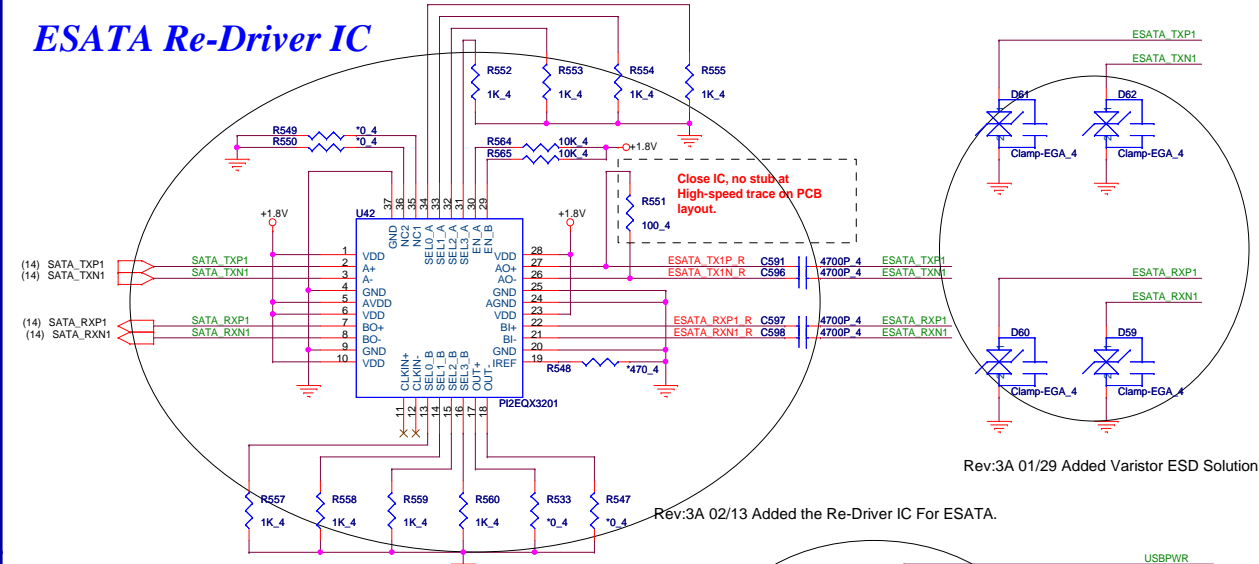


Rev:3A 01/29 Added Varistor ESD Solution.

USB & ESATA



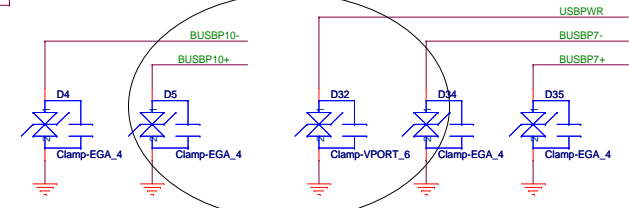
ESATA Re-Driver IC



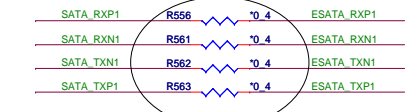
Rev:3A 01/29 Added Varistor ESD Solution.

Rev:3A 02/13 Added the Re-Driver IC For ESATA.

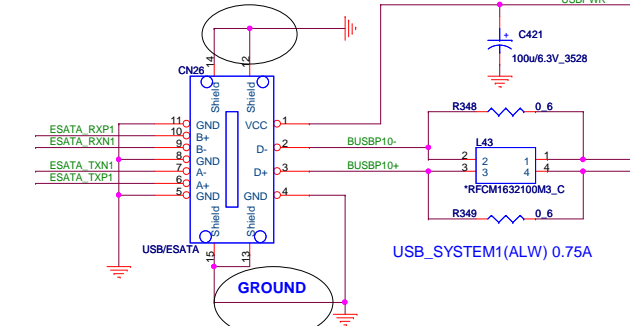
SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				



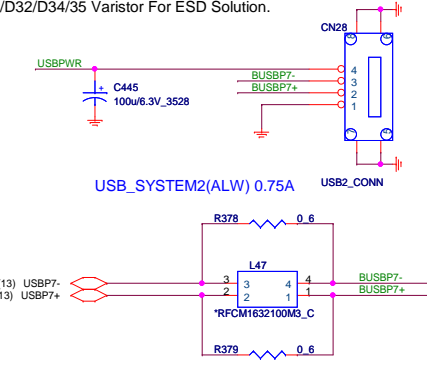
Rev:3A 03/03 Stuff the D4/D5/D32/D34/35 Varistor For ESD Solution.



Rev:3A 02/05 Added PIN12/14 To Ground For ESD.

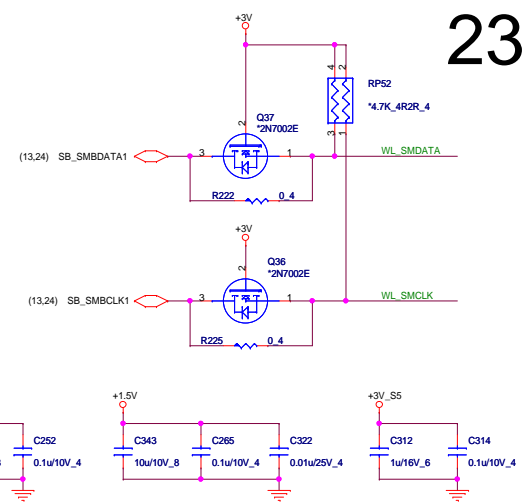
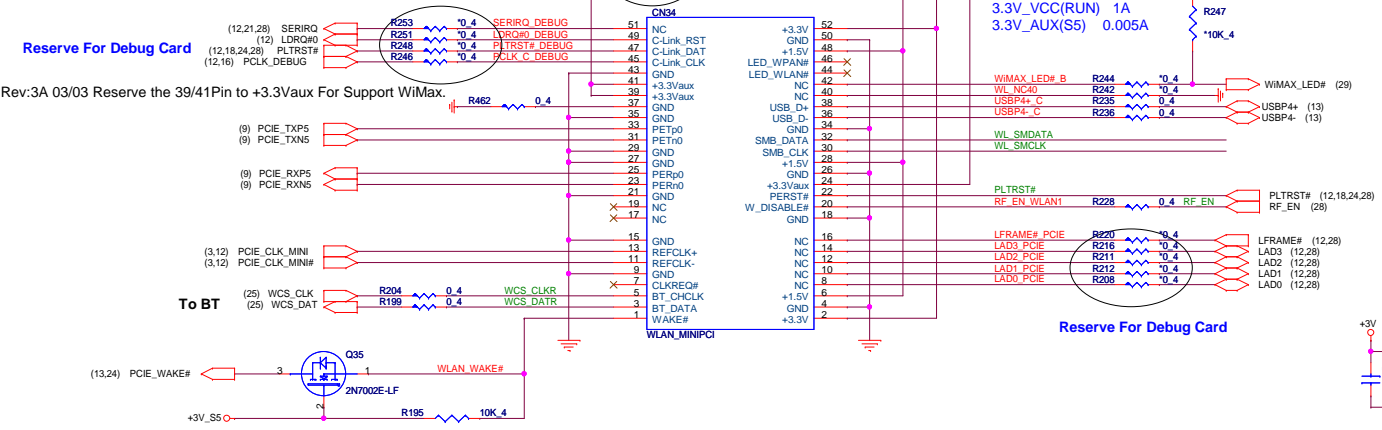


Rev:3A 01/29 Delete R133 For ESD Solution.

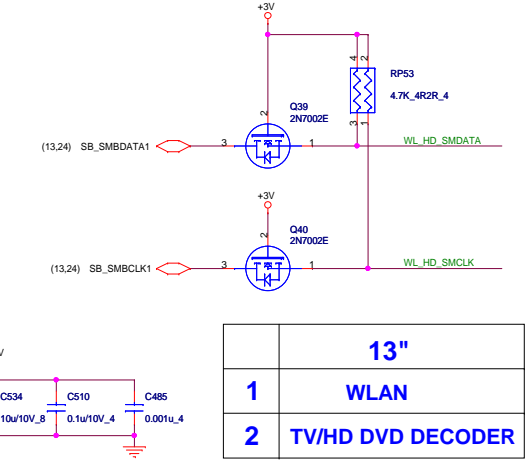
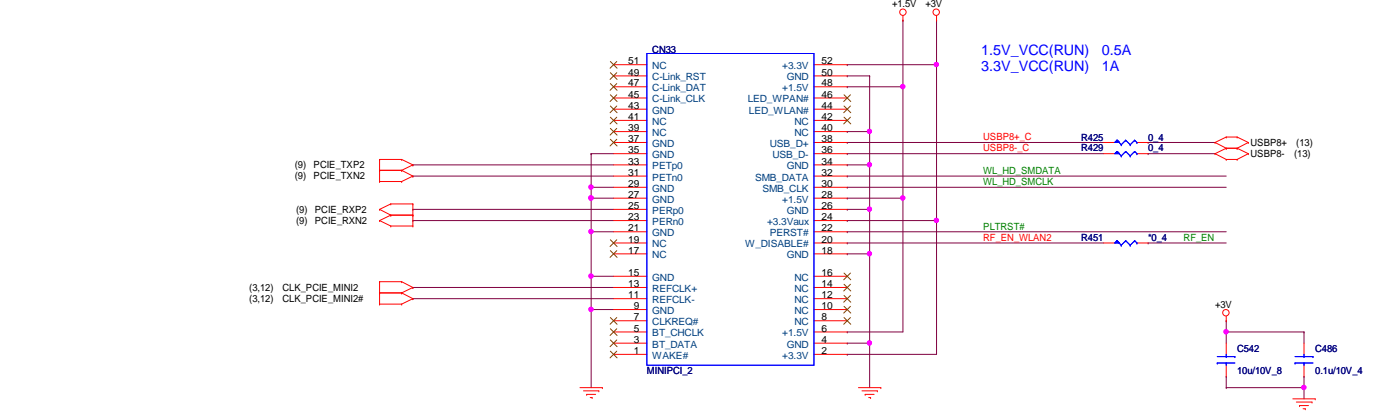


	PROJECT : BU2	
	Quantal Computer Inc.	
	Size Custom Document Number SATA HDD/ODD & ESATA/USB	Date: Tuesday, August 19, 2008

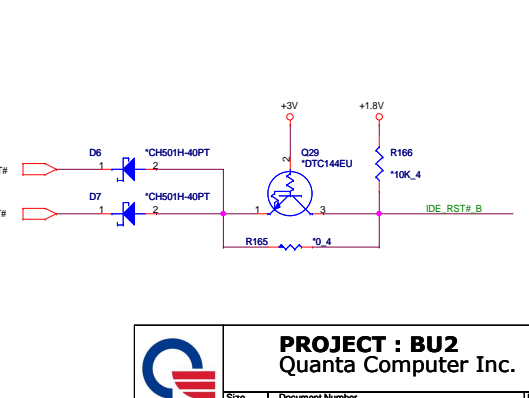
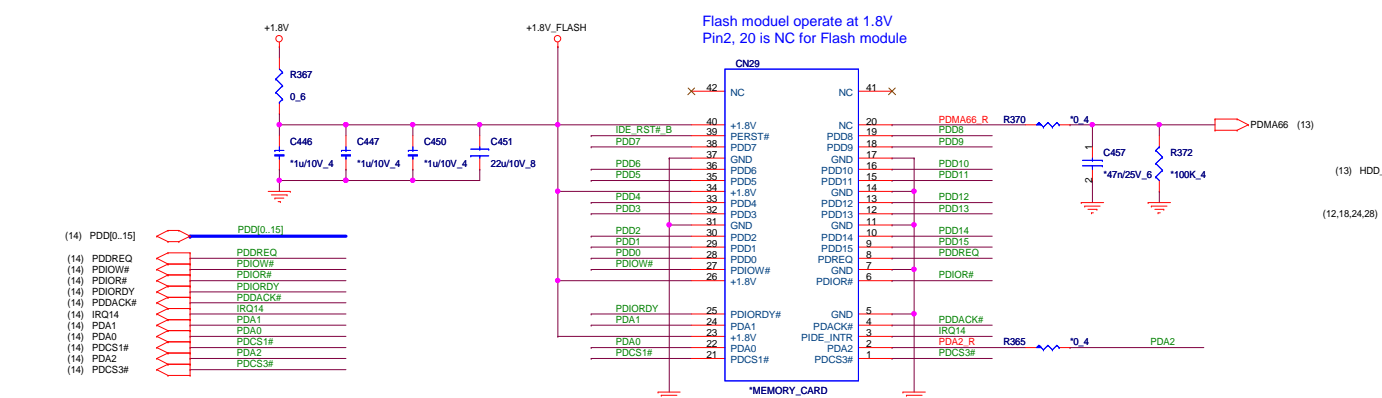
MINI CARD 1 5.6H_WLAN



MINI Card 2 5.6H_TV/HD DVD DECODER



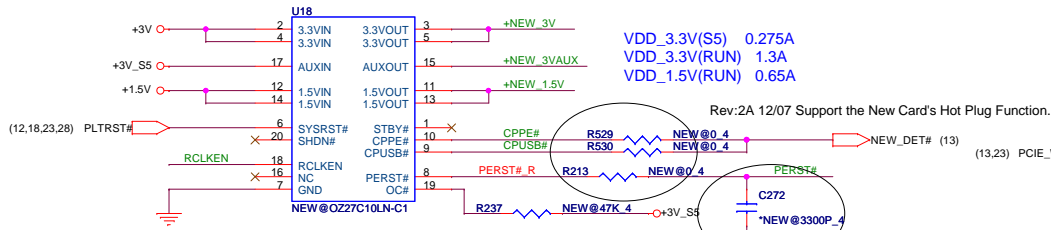
NAND FLASH MEMORY CARD



PROJECT : BU2
Quanta Computer Inc.

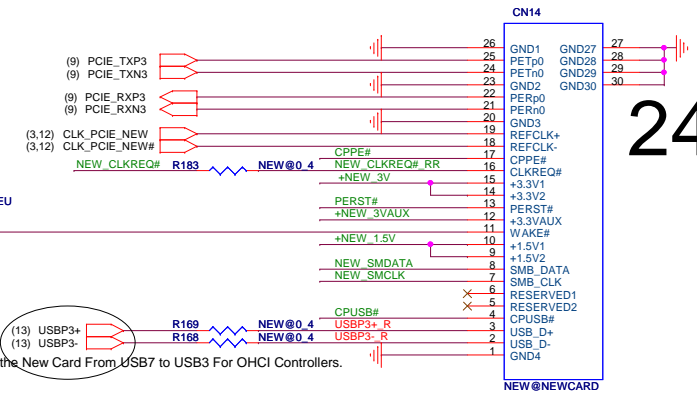
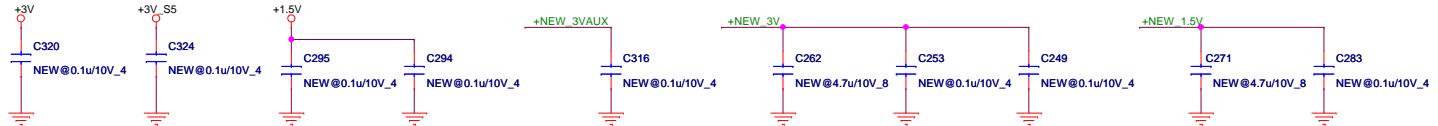
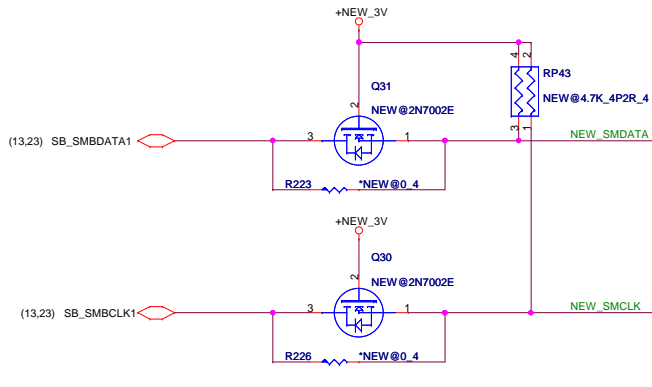
Size Custom	Document Number MINI CARD & NAND FLASH CARD	Rev 1A
Date: Thursday, July 24, 2008		Sheet 23 of 35

NEW CARD(BTO)

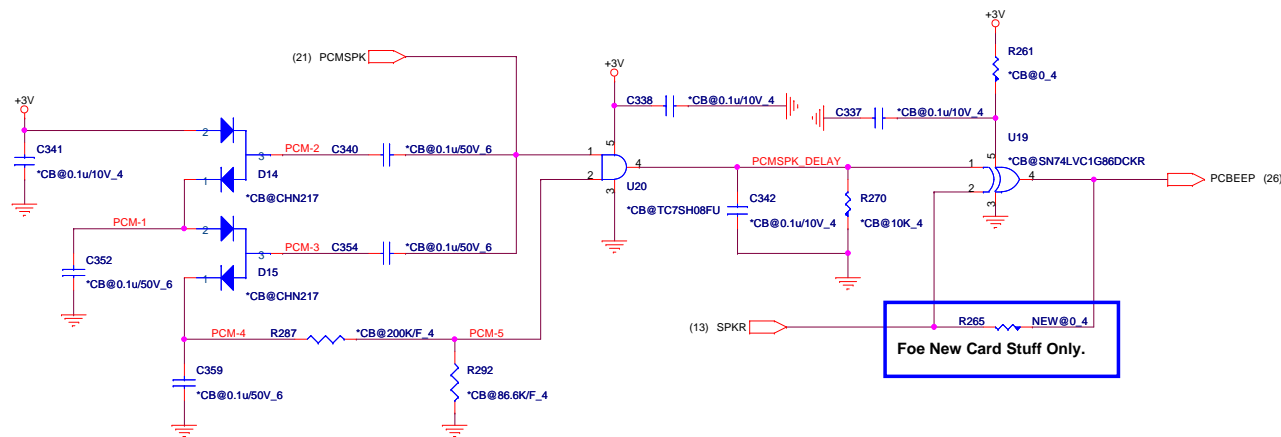


NEW CARD'S POWER SWITCH

Rev:3A 03/03 As check with AE regarding to PERST# do not add any delay into PERST#

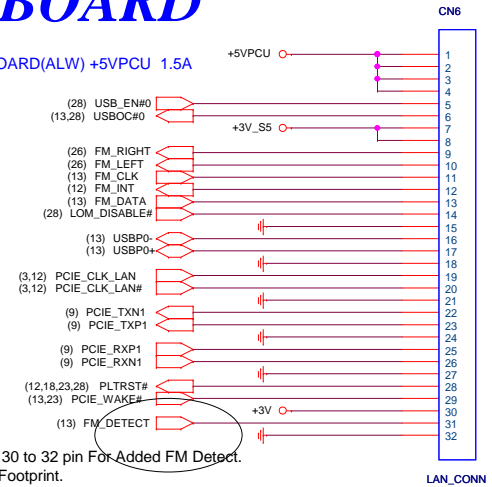


PC-BEEP



RJ45/USB BOARD

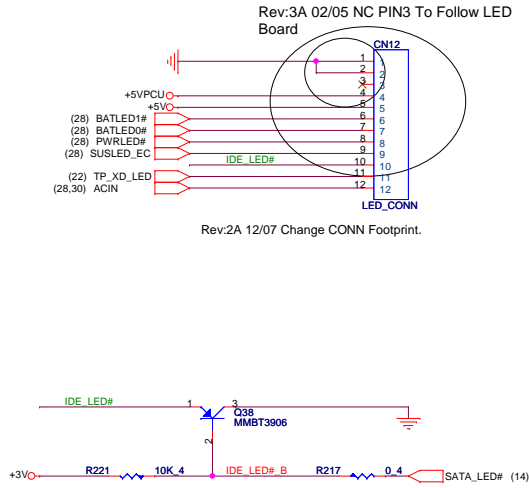
USB & LAN BOARD(ALW) +5VPCU 1.5A



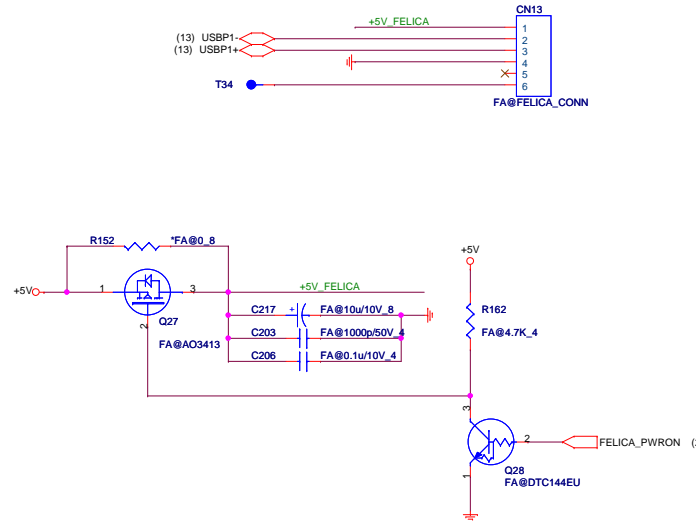
PROJECT : BU2
Quanta Computer Inc.

Size Custom Document Number **NEW CARD & RJ45 BOARD/BEEP** Rev 1A
Date: Thursday, July 24, 2008 Sheet 24 of 35

LED BOARD

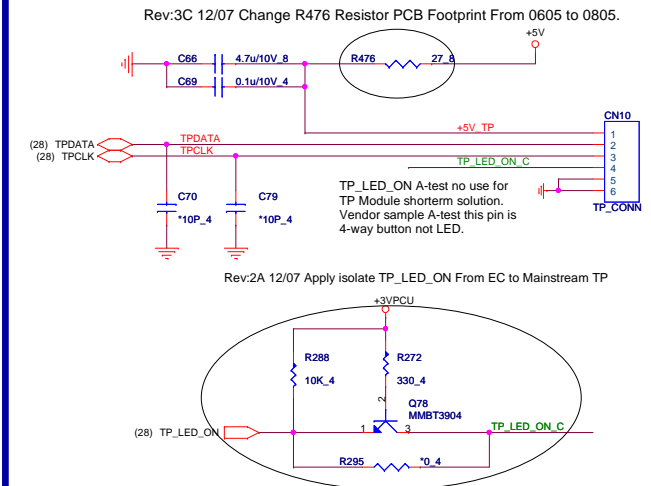


Felica

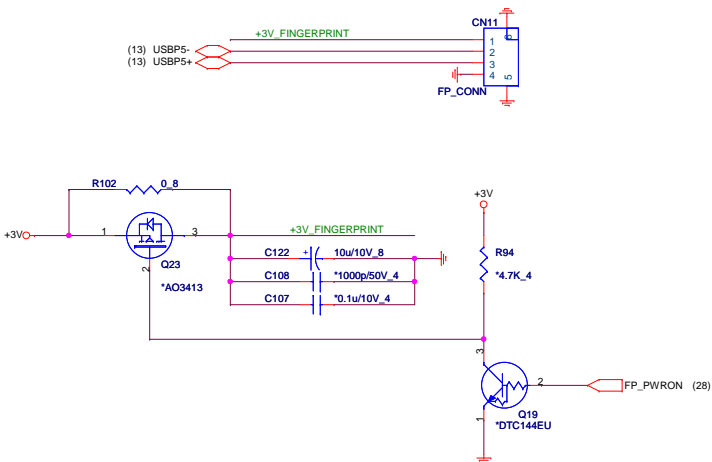


TP BOARD

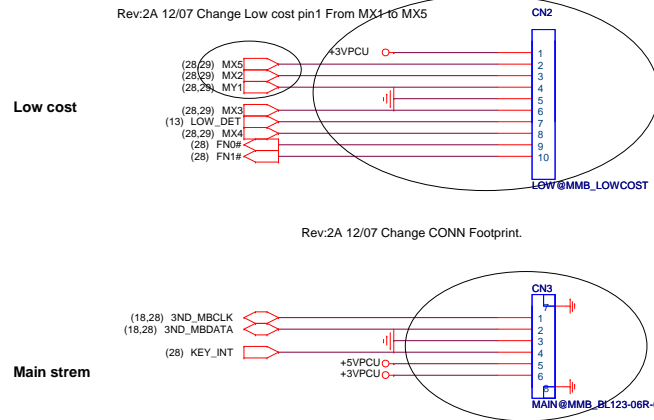
25



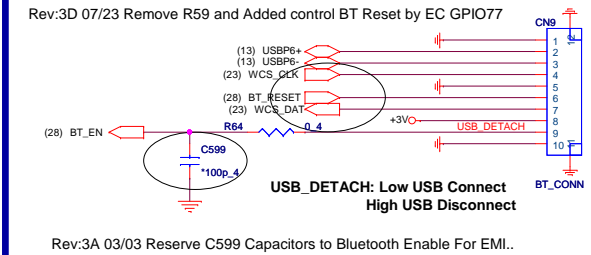
FINGER-PRINT



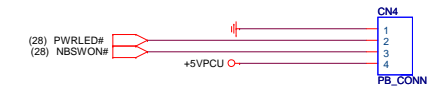
MMB



Bluetooth Module



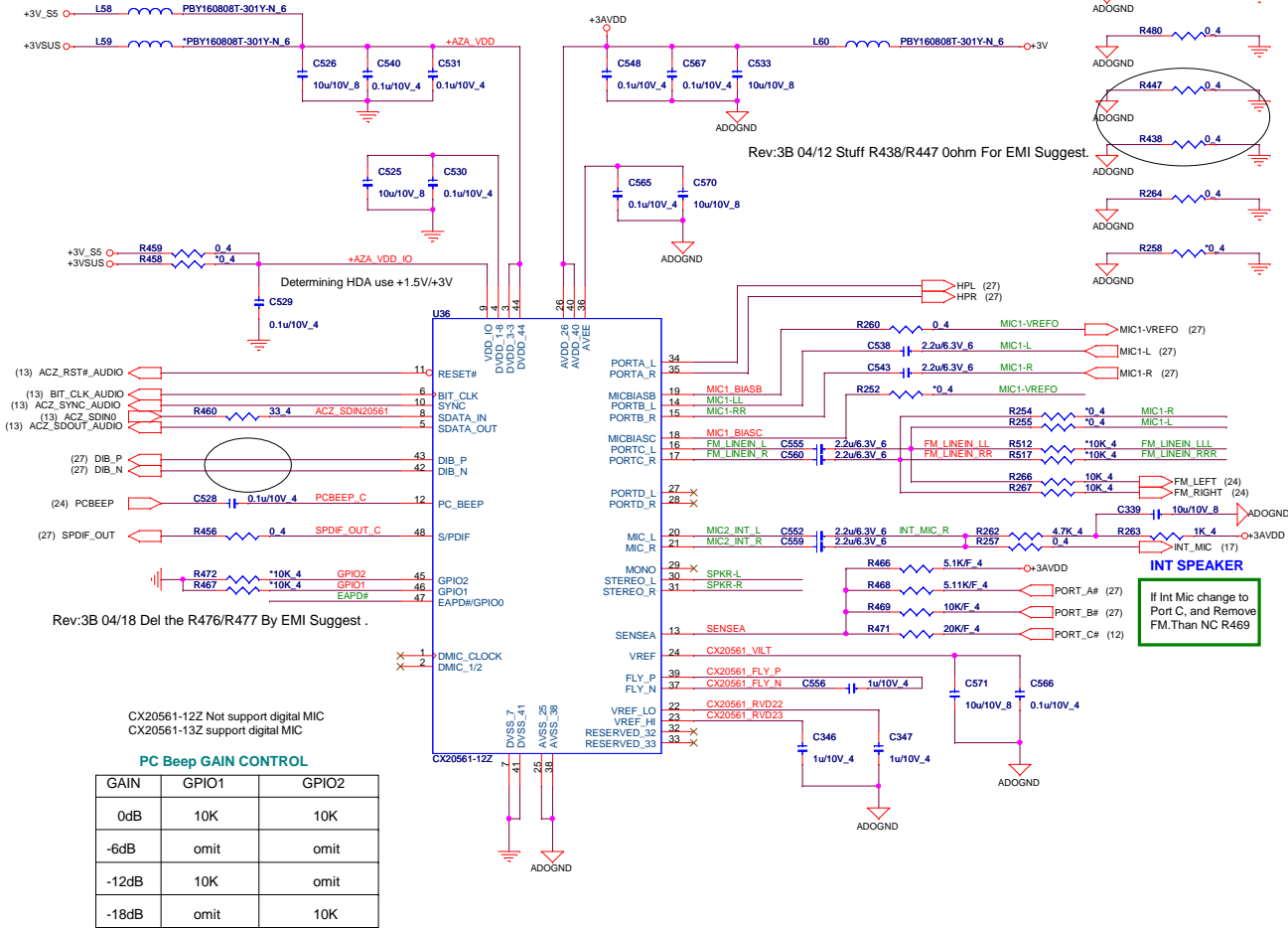
POWER BOARD



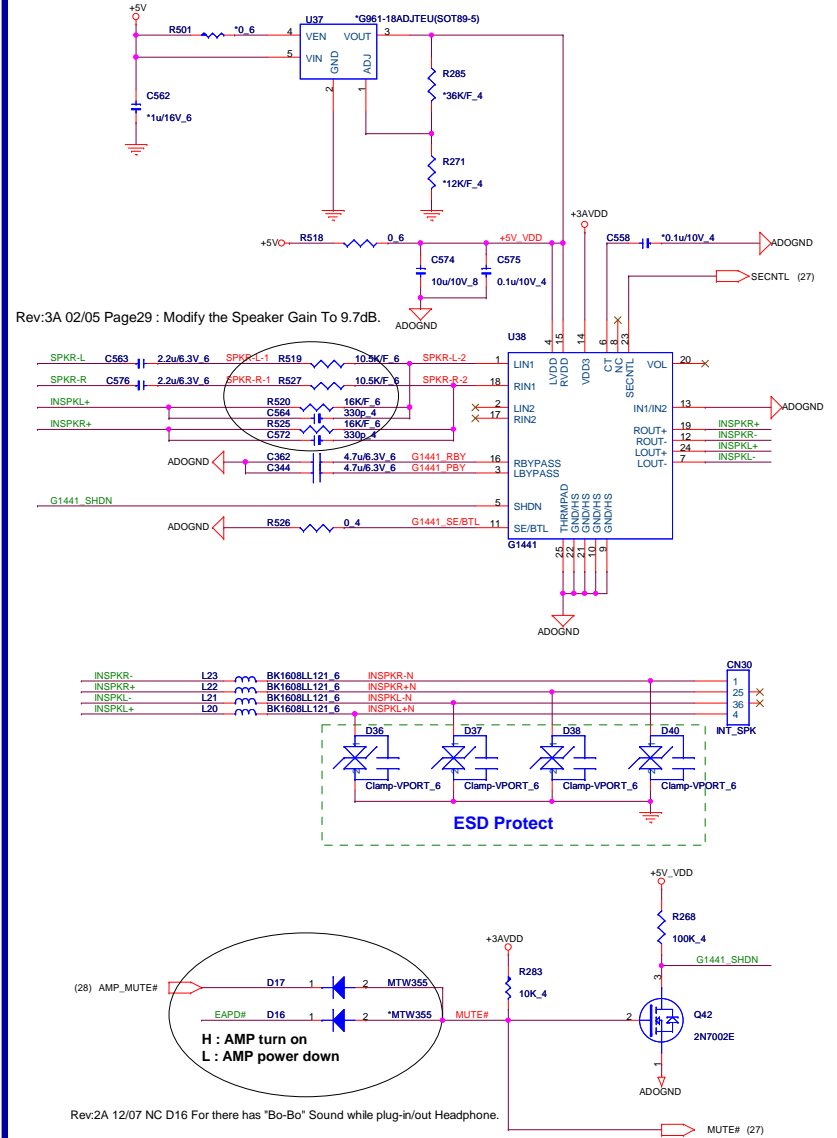
	PROJECT : BU2		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	TP/FP/BT/PB/FELICA/MMB CONN	Sheet 25 of 35
NB4	Date: Tuesday, August 19, 2008		

CODEC(CX20561)

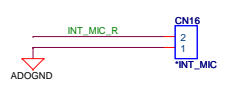
Rev:3A 02/05 Added the EMI Solution.



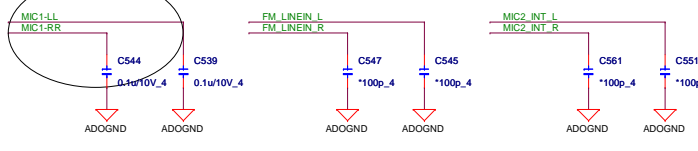
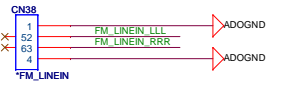
INT SPK AMP



Reserve INTMIC

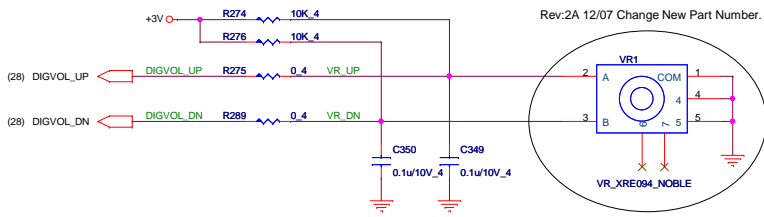


Reserve FM

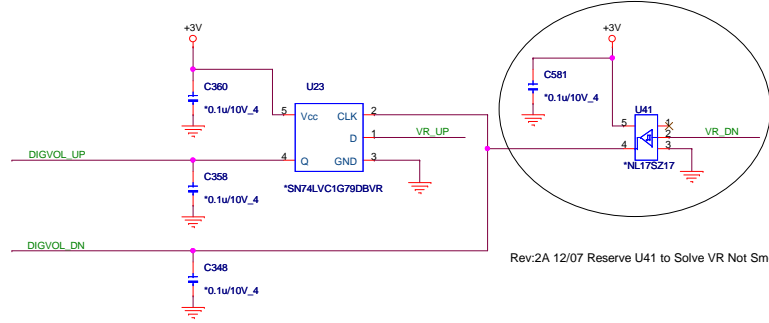


PROJECT : BU2
Quanta Computer Inc.

Size Custom	Document Number CONEXANT(CX205601)/SPK/AMP	Rev 1A
Date: Thursday, July 24, 2008		Sheet 26 of 35

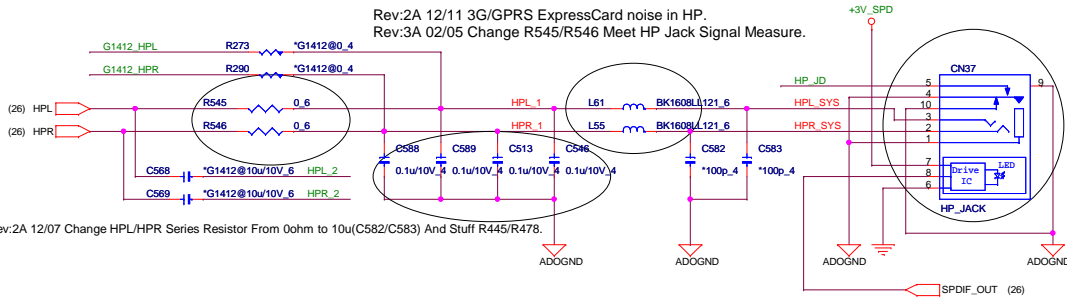


Rev:2A 12/07 Change New Part Number.



Rev:2A 12/07 Reserve U41 to Solve VR Not Smooth.

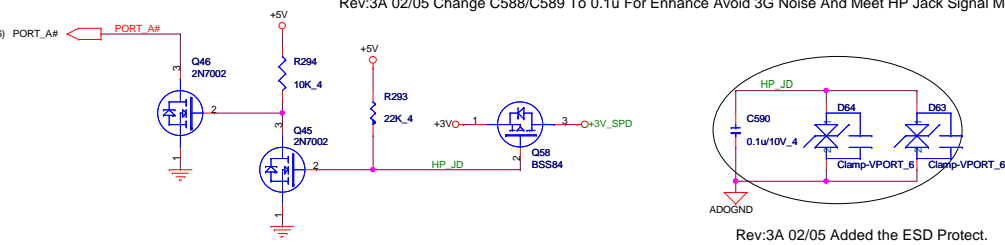
HP JACK



Rev:2A 12/11 3G/GPRS ExpressCard noise in HP.
Rev:3A 02/05 Change R545/R546 Meet HP Jack Signal Measure.

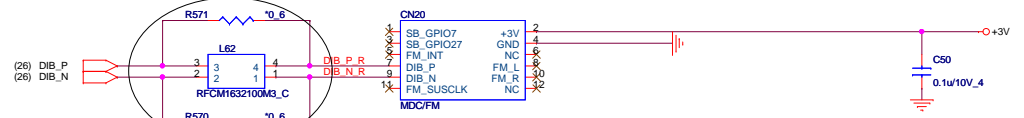
Rev:2A 12/07 Change HPL/HPR Series Resistor From 0ohm to 10u(C582/C583) And Stuff R445/R478.

Rev:2A 12/13 CN37 9/10# Shield Pin to ADGND For ESD issue.
Rev:3A 02/05 Change C588/C589 To 0.1u For Enhance Avoid 3G Noise And Meet HP Jack Signal Measure



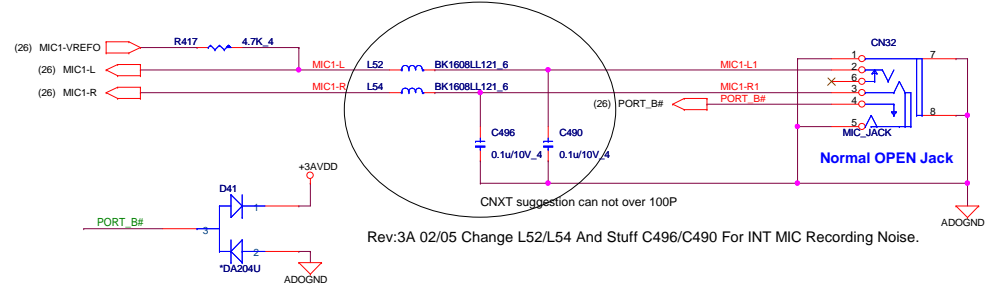
Rev:3A 02/05 Added the ESD Protect.

FM TUNER & MDC



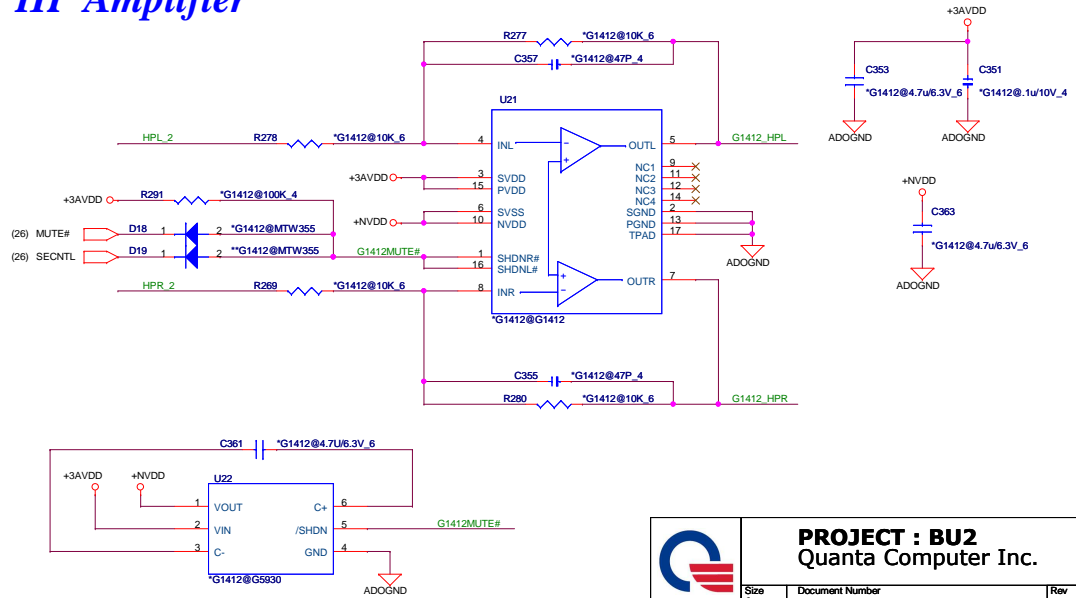
Rev:3B 04/18 Added the common mode choke on DIB_P/N For EMI Solution.

SYSTEM MIC



Rev:3A 02/05 Change L52/L54 And Stuff C496/C490 For INT MIC Recording Noise.

HP Amplifier



NB4	PROJECT : BU2			Rev 1A
	Quanta Computer Inc.			
Size Custom	Document Number JACK/VR/FM/MIC/MDC/AMPLIFIER			
Date: Thursday, July 24, 2008	Sheet	27	of	35

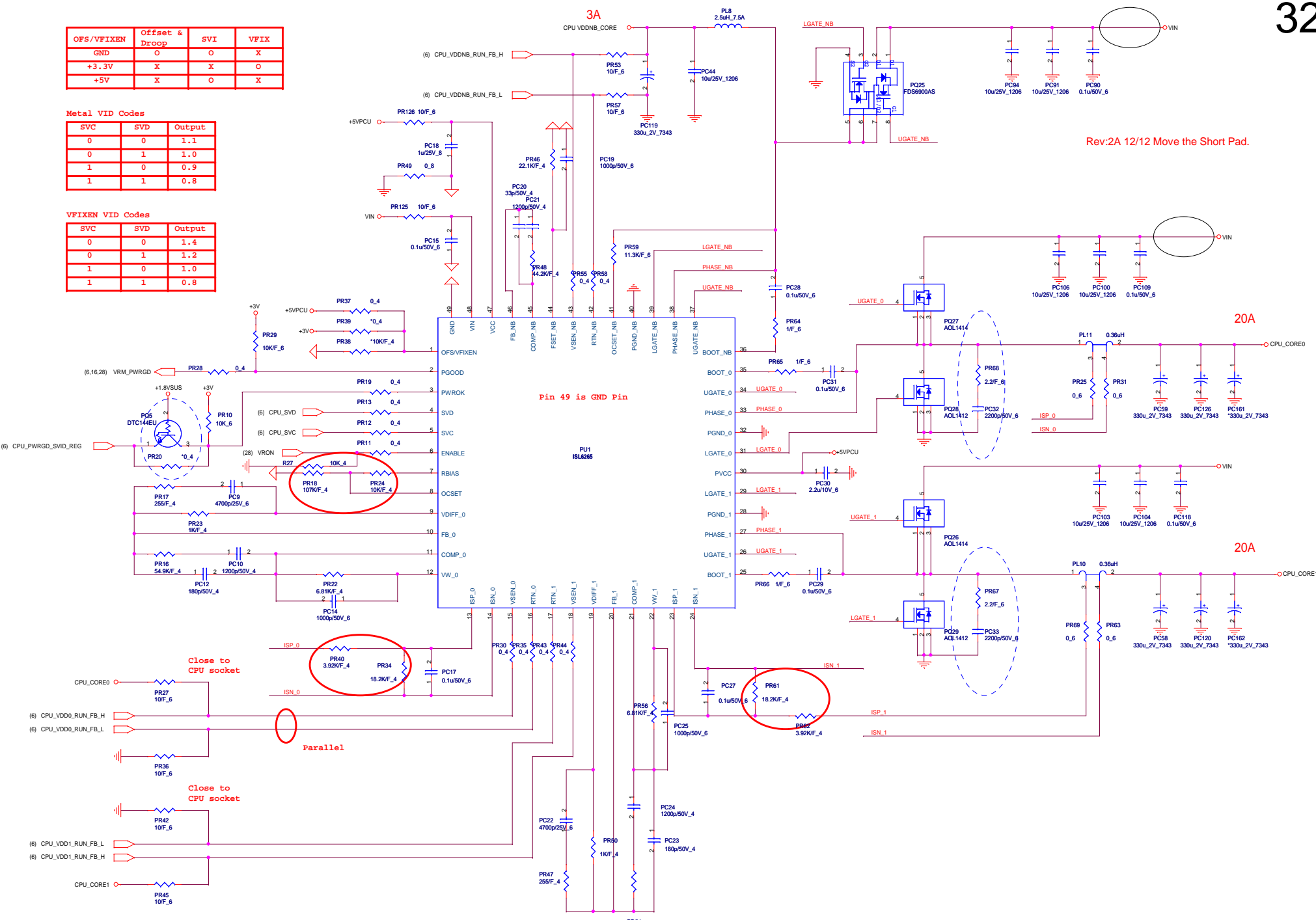
OFS/VFIXEN	Offset & Droop	SVC	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

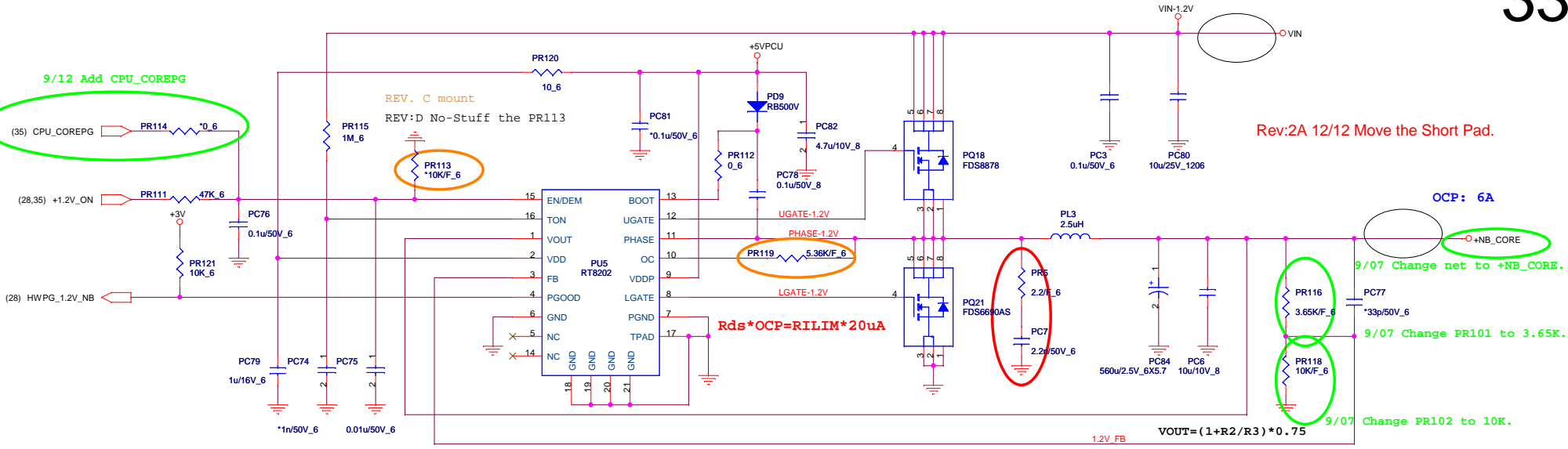
Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





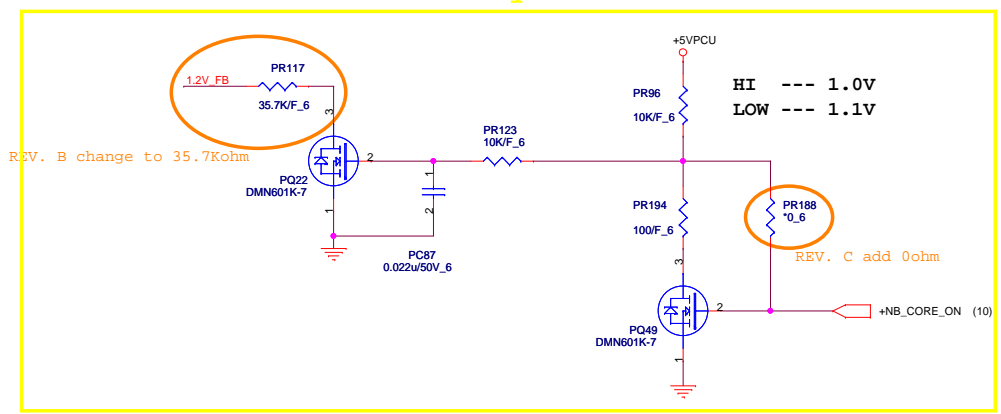
$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$
 $Frequency = V_{out} / (V_{in} * T_{ON})$

6A OCP --- $OC = 4.53K$
FDS6690AS $R_{ds} = 15m\Omega$

REV. C PR119 change to 5.36Kohm

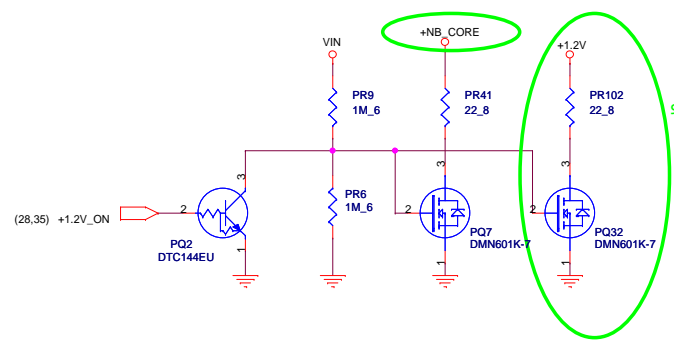
$V_{OUT} = (1 + R2/R3) * 0.75$

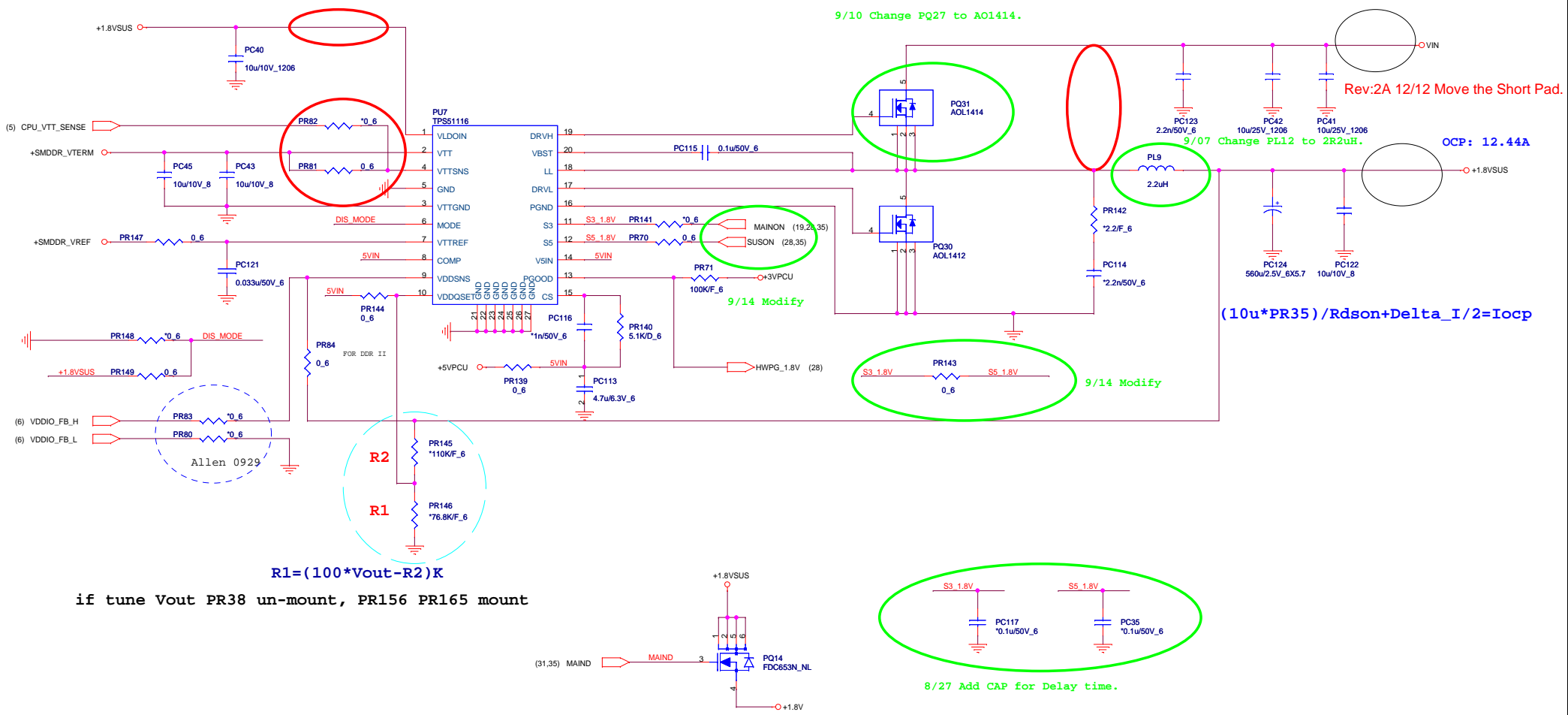
1/30 modify



9/07 Change net to +NB_CORE.

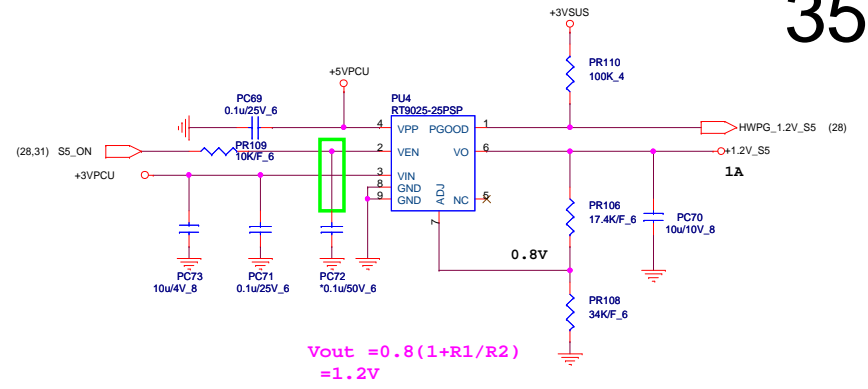
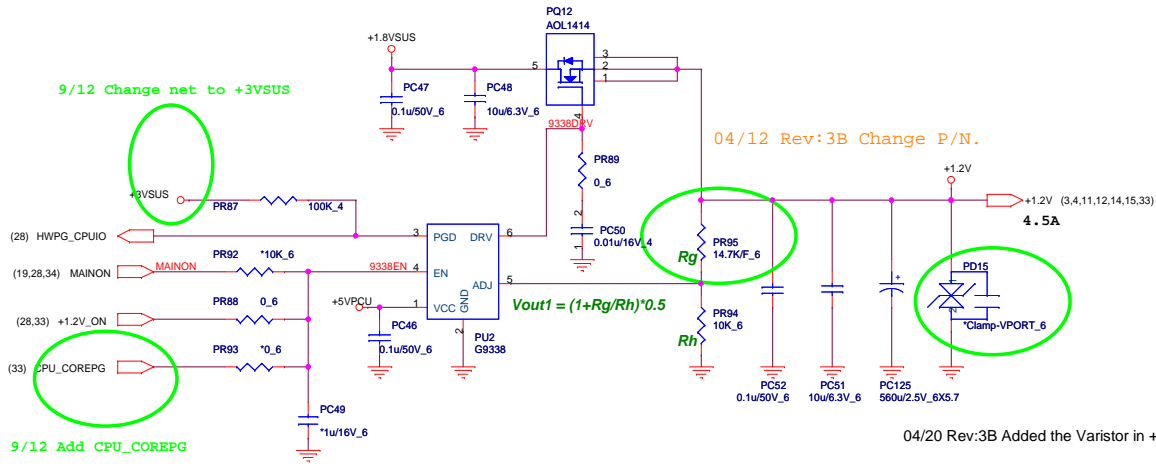
9/12 Addition PR156, PQ43.





$R1 = (100 * V_{out} - R2) / K$

if tune Vout PR38 un-mount, PR156 PR165 mount



04/20 Rev:3B Added the Varistor in +1.2V Domain.

